YAMAHA

YDA142

D-3D

DIGITAL INPUT STEREO 9.5W DIGITAL AUDIO POWER AMPLIFIER

■Overview

YDA142 (D-3D) is a 12V single supply voltage, high-efficiency digital audio power amplifier IC.
An audio power amplifier with a maximum output of 9.5W (R_L=8Ω) × 2ch or 19W (R_L=4Ω) × 1ch can be configured with one chip.
YDA142 has a "Pure Pulse Direct Speaker Drive Circuit" that directly drives speakers while reducing distortion of a pulse output signal and reducing noise on a signal, and it realizes the highest standard low distortion rate characteristics and low noise characteristics as compared with those of digital amplifier ICs in the same class. The circuit allows you to design a circuit with as few external parts as possible depending on use conditions because any filter is no longer required.
It is possible to input a left-justified or right-justified 16bit/8bit digital audio signal of 32kHz, 44.1kHz, or 48kHz.
In addition, YDA142 has a gain setting function in 32-level (analog setting) or 8-level (terminal setting).
YDA142 has Over-current Protection function for speaker output terminals, IC Thermal Protection function, POP Noise Reduction function, and DC Input Detection function as well as Power-down function and Output Disable function.

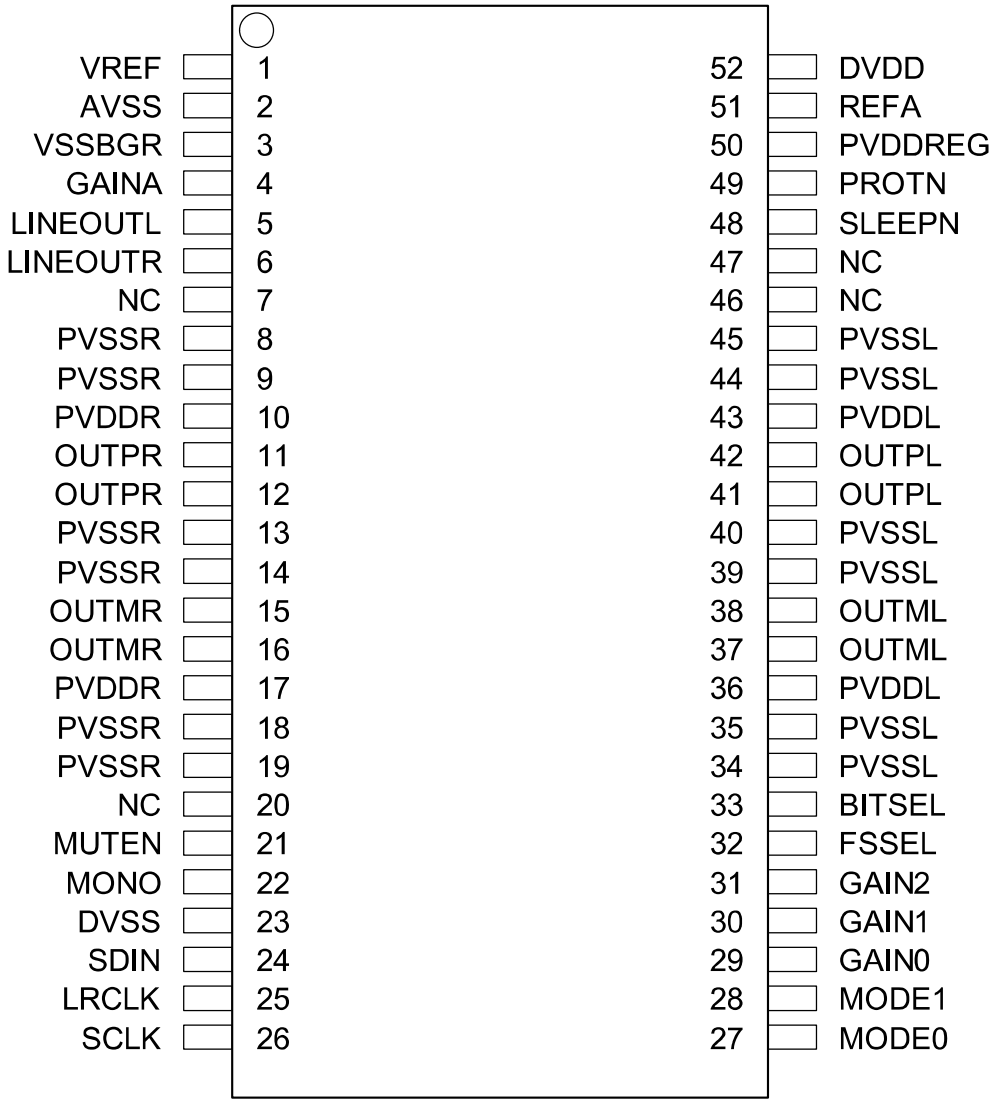
■Features

・Maximum Output
  9.5 W×2ch (V_{DDP}=12.0V, R_L=8Ω, THD+N=10%, MONO=L, GAIN[2:0]=H,L,L)
  19 W×1ch (V_{DDP}=12.0V, R_L=4Ω, THD+N=10%, MONO=H, GAIN[2:0]=H,L,L)
・Efficiency
  90 % (V_{DDP}=12.0V, R_L=8Ω, Po=9.5W)
・Distortion Rate (THD+N)
  0.05 % (V_{DDP}=12.0V, R_L=8Ω, Po=1.0W, GAIN[2:0]=H,L,L)
・S/N Ratio
  100dB (V_{DDP}=12.0V, R_L=8Ω, Po=9.5W, GAIN[2:0]=H,L,L)
・Channel Separation Ratio
  -78dB (V_{DDP}=12.0V)
・Supply voltage Range
  9.0V to 13.5V
・3-wire Digital Signal Input
  Fs: 32kHz/44.1kHz or 48kHz, Bits: 16bit or 18bit
・Gain Setting Function with GAIN[2:0] and GAINA terminal
・Power-down Function with SLEEPN terminal
・Output Mute Function with MUTEN terminal
・Monaural Output Function with MONO terminal
・Protection Functions (Over-current Protection, Thermal Protection, Clock Stop protection, Under-voltage Malfunction Prevention, DC Input Detection)
・Pop-noise Reduction Function
・Digital Input/BTL(Bridge-Tied Load) output
・Package
  Lead-free 52-pin SSOP (YDA142-EZ)

YAMAHA CORPORATION

YDA142 CATALOG
CATALOG No.:LSI-4DA142A20
2006.4

■Terminal configuration



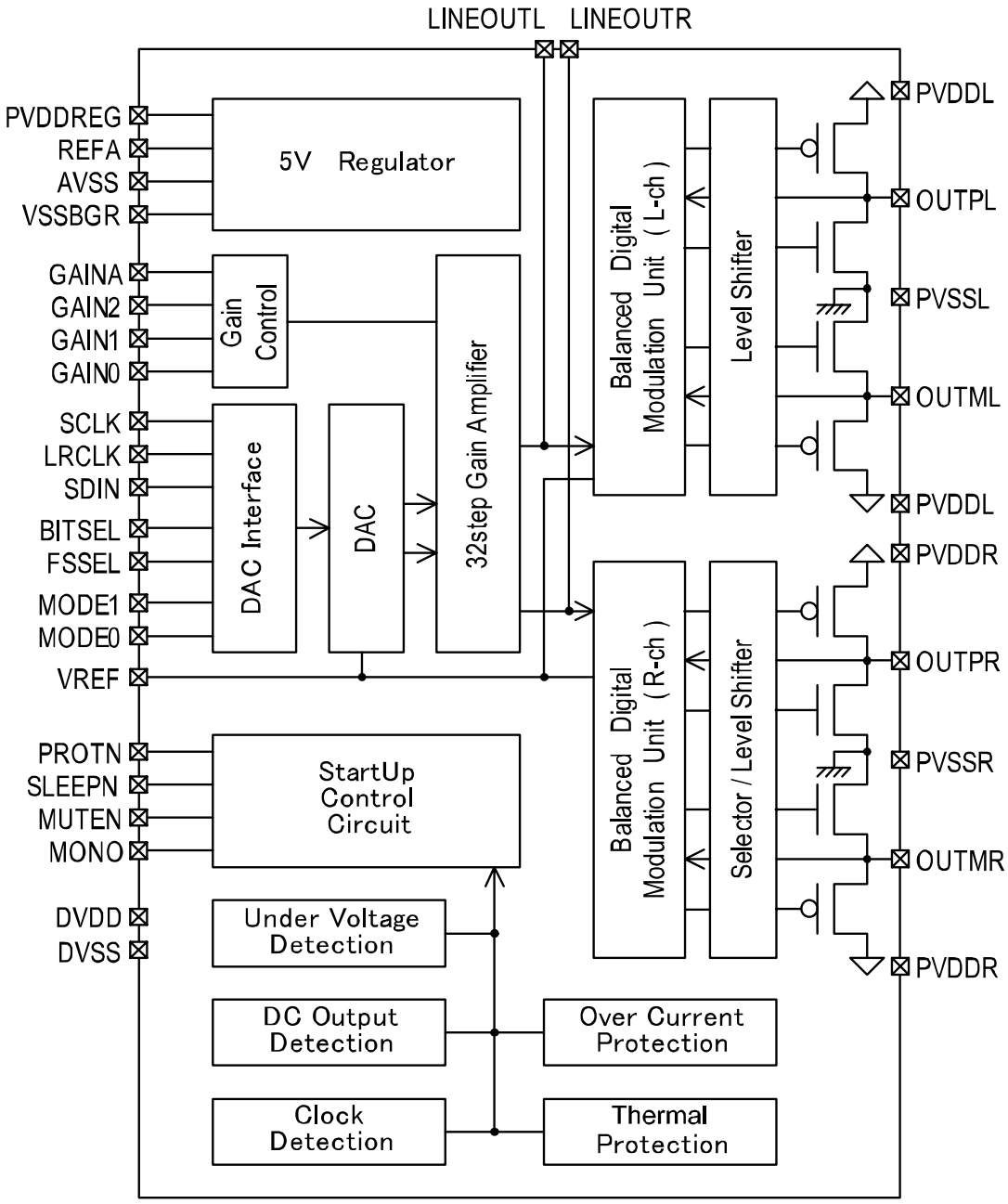
<52-pin SSOP Top View>

■Terminal function

No.	Name	I/O	Function	Voltage tolerance
1	VREF	O	Analog reference voltage output	LV
2	AVSS	GND	Ground terminal for analog circuits	−
3	VSSBGR	GND	Ground terminal for analog circuits	−
4	GAINA	I	Analog gain setting terminal	LV
5	LINEOUTL	O	Lch Line output terminal	LV
6	LINEOUTR	O	Rch Line output terminal	LV
7	NC	−	Normally, use this terminal in no-connection	−
8	PVSSR	GND	Ground terminal	−
9	PVSSR	GND	Ground terminal	−
10	PVDDR	Power	12V power supply terminal	HV
11	OUTPR	O	Rch positive side output terminal	HV
12	OUTPR	O	Rch positive side output terminal	HV
13	PVSSR	GND	Ground terminal	−
14	PVSSR	GND	Ground terminal	−
15	OUTMR	O	Rch negative side output terminal	HV
16	OUTMR	O	Rch negative side output terminal	HV
17	PVDDR	Power	12V power supply terminal	HV
18	PVSSR	GND	Ground terminal	−
19	PVSSR	GND	Ground terminal	−
20	NC	−	Normally, use this terminal in no-connection	−
21	MUTEN	I	Output disable control terminal	LV
22	MONO	I	Monaural control terminal	LV
23	DVSS	GND	Ground terminal for digital circuits	−
24	SDIN	I	Serial audio data signal input	LV
25	LRCLK	I	Serial LR clock signal input	LV
26	SCLK	I	Serial bit clock signal input	LV
27	MODE0	I	Mode setting terminal 0	LV
28	MODE1	I	Mode setting terminal 1	LV
29	GAIN0	I	Volume setting terminal 0	LV
30	GAIN1	I	Volume setting terminal 1	LV
31	GAIN2	I	Volume setting terminal 2	LV
32	FSSEL	I	Sampling frequency setting terminal	LV
33	BITSEL	I	16bit/18bit setting terminal	LV
34	PVSSL	GND	Ground terminal	−
35	PVSSL	GND	Ground terminal	−
36	PVDDL	Power	12V power supply terminal	HV
37	OUTML	O	Lch negative side output terminal	HV
38	OUTML	O	Lch negative side output terminal	HV
39	PVSSL	GND	Ground terminal	−
40	PVSSL	GND	Ground terminal	−
41	OUTPL	O	Lch positive side output terminal	HV
42	OUTPL	O	Lch positive side output terminal	HV
43	PVDDL	Power	12V power supply terminal	HV
44	PVSSL	GND	Ground terminal	−
45	PVSSL	GND	Ground terminal	−
46	NC	−	Normally, use this terminal in no-connection	−
47	NC	−	Normally, use this terminal in no-connection	−
48	SLEEPN	I	Power-down control terminal	HV
49	PROTN	O/D	Unusual condition warning output terminal	HV
50	PVDDREG	Power	12V power supply terminal for analog circuits	HV
51	REFA	O	5V reference voltage output terminal	LV
52	DVDD	I	5V reference voltage input terminal	LV

（Note） I: Input terminal, O: Output terminal, O/D: Open drain output terminal
LV: Terminal for V_{REG} power supply voltage range as input voltage range.
HV: Terminal for V_{DDP} power supply voltage range as input voltage range.

■Block diagram



■Description of operating functions

●Serial Audio Interface

Sampling Frequency (Fs) Selection

Input an audio signal using SCLK, LRCLK, and SDIN terminals. YDA142 supports three sampling frequencies (Fs): 32kHz, 44.1kHz, and 48kHz. Set the FSSEL terminal as follows in accordance with a Fs of a signal to use. At this time, use a frequency of 64Fs as a SCLK signal.

FSSEL terminal setting

FSSEL	Sampling Frequency (Fs)
L	44.1kHz, 48kHz
H	32kHz

Bit Number Selection

YDA142 supports two bit widths: 16-bit and 18-bit. Set the BITSEL terminal as follows in accordance with a bit width to use.

BITSEL terminal setting

BITSEL	Input Bit Number
L	16 bits
H	18 bits

Format Selection

YDA142 can select one out of three interface formats: Right-justified MSB first format, Left-justified MSB first format, and Left-justified (1bit delay) MSB first format. Set the MODE[1:0] as follows in accordance with a digital audio signal format to use. Fig.1 to Fig.3 shows the details of each format.

MODE[1:0] terminal setting

MODE1	MODE0	Input Signal Format
L	L	Right-justified MSB first
L	H	Left-justified MSB first
H	L	Left-justified (1bit delay) MSB first
H	H	Reserved

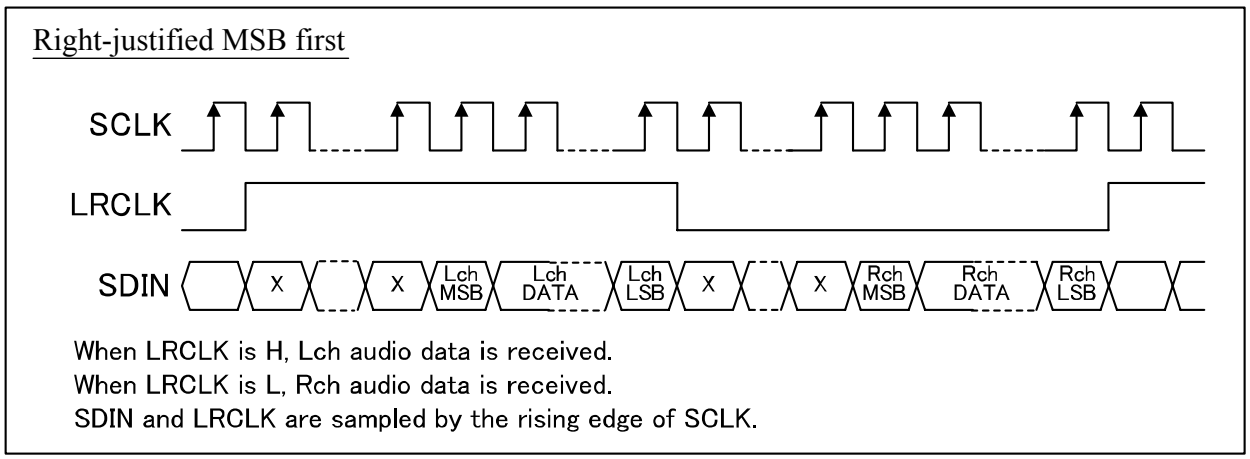


Fig.1 Right-justified MSB First Format

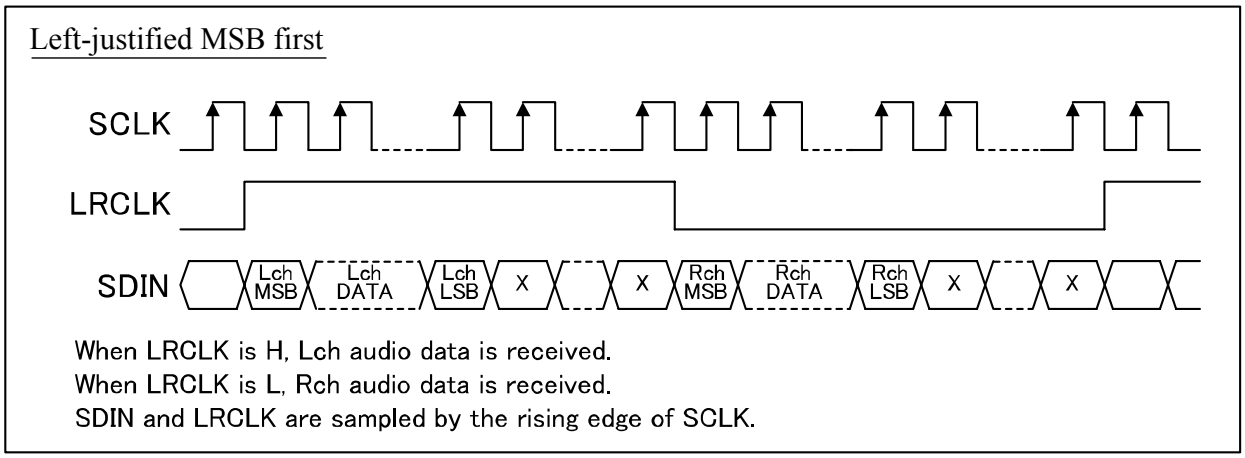


Fig.2 Left-justified MSB First Format

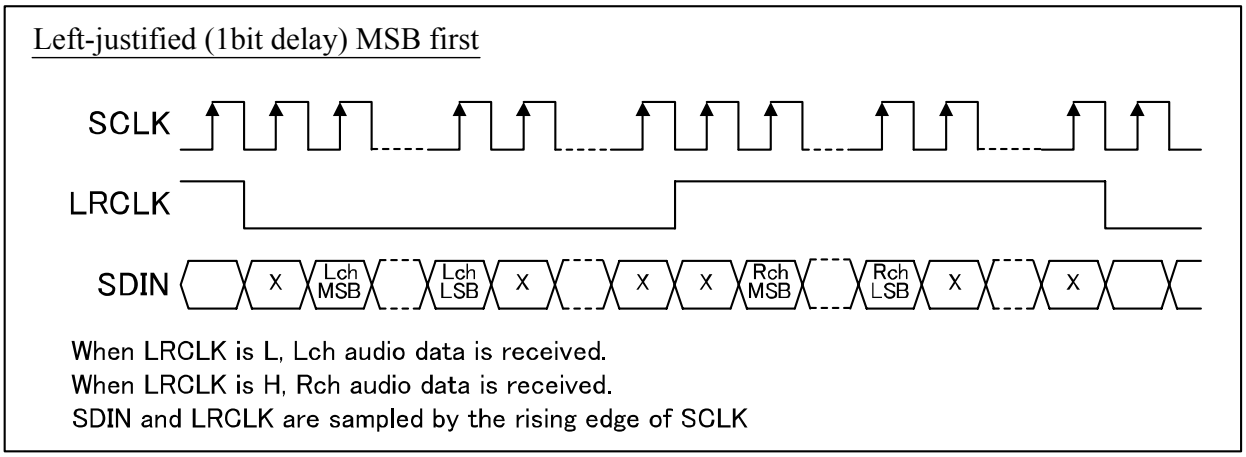


Fig.3 Left-justified (1bit delay) MSB First Format

●Gain setting function

The output gain for a digital amplifier and LINEOUTL(R) can be set by GAIN[2:0] terminal and GAINA terminal.
Set the GAIN[2:0] as follows in accordance with a gain to use.
With GAIN[2:0]= "L, L, L" the output gain of a digital amplifier and LINEOUTL(R) can be set by a GAINA terminal voltage. Set the GAINA terminal voltage as follows in accordance with a gain to use.
When the GAINA terminal is not used, it is fixed to GND.

GAIN[2:0] terminal gain setting

GAIN2	GAIN1	GAIN0	Digital Amplifier Gain	LINEOUTL(R) Output Gain
L	L	L	GAINA terminal priority	GAINA terminal priority
L	L	H	2dB	-15dB
L	H	L	8dB	-9dB
L	H	H	14dB	-3dB
H	L	L	20dB	3dB
H	L	H	23dB	6dB
H	H	L	26dB	9dB
H	H	H	29dB	12dB

GAINA terminal Gain setting

GAINA terminal voltage range (Voltage ratio to REFA voltage)			Digital Amplifier Gain	LINEOUTL(R) Output Gain
65.6%	to	100.0%	32dB	15dB
64.0%	to	67.2%	29dB	12dB
62.4%	to	65.6%	26dB	9dB
60.8%	to	64.0%	23dB	6dB
59.2%	to	62.4%	20dB	3dB
57.6%	to	60.8%	18dB	1dB
56.0%	to	59.2%	16dB	-1dB
54.4%	to	57.6%	14dB	-3dB
52.8%	to	56.0%	12dB	-5dB
51.2%	to	54.4%	10dB	-7dB
49.6%	to	52.8%	8dB	-9dB
48.0%	to	51.2%	6dB	-11dB
46.4%	to	49.6%	4dB	-13dB
44.8%	to	48.0%	2dB	-15dB
43.2%	to	46.4%	0dB	-17dB
41.6%	to	44.8%	-2dB	-19dB
40.0%	to	43.2%	-4dB	-21dB
38.4%	to	41.6%	-6dB	-23dB
36.8%	to	40.0%	-8dB	-25dB
35.2%	to	38.4%	-10dB	-27dB
33.6%	to	36.8%	-12dB	-29dB
32.0%	to	35.2%	-14dB	-31dB
30.4%	to	33.6%	-16dB	-33dB
28.8%	to	32.0%	-18dB	-35dB
27.2%	to	30.4%	-20dB	-37dB
25.6%	to	28.8%	-23dB	-40dB
24.0%	to	27.2%	-26dB	-43dB
22.4%	to	25.6%	-29dB	-46dB
20.8%	to	24.0%	-32dB	-49dB
19.2%	to	22.4%	-36dB	-53dB
17.6%	to	20.8%	-40dB	-57dB
0%	to	19.2%	Mute	Mute

A full scale of DAC is 1Vrms(2.8Vpp). This is assumed to be 0dB and the gain is set.
For instance, when the gain of a digital amplifier is set to 14dB, and a full-scale signal of DAC is input, the digital amplifier output becomes 5Vrms(14Vpp).

●Analog Signal Output

When SLEEPN terminal is “H”, L channel and R channel analog signals are output from LINEOUTL terminal and LINEOUTR terminal respectively, with an output gain designated by GAIN[2:0] terminal or GAINA terminal with respect to an input digital signal.
The DC component is superimposed and output from LINEOUTL and LINEOUTR terminal. Therefore, the DC component is removed with the DC cut capacitor.

●Digital Amplifier Output

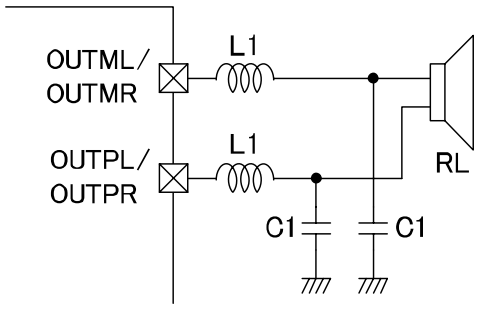
When SLEEPN terminal is “H” and MUTEN terminal is “H”, L channel signal is output between OUTPL terminal and OUTML terminal, with an output gain designated by GAIN[2:0] terminal or GAINA terminal with respect to an input digital signal. In addition, R channel signal is output between OUTPR terminal and OUTMR terminal. OUTPL and OUTPR terminal become a positive terminal, and OUTML and OUTMR terminals become a minus terminal, respectively.

LC Filter

YDA142 can be directly connected to a speaker without a LC filter because it adopts a modulation method capable of reducing speaker loss during no sound sufficiently by utilizing only inductance a speaker has. When a LC filter is not used, use a speaker with inductance of 20μH or over at a carrier clock frequency of 500kHz.
Use the following filter circuit when a LC filter is connected. At this time, use the following constants in accordance with speaker's impedance. Using these constants can make a low-pass filter with a cut-off frequency of 50kHz, Q=0.7 or so.
The over current protection function might work by LC resonance when the LC filter is connected and uses, and operate IC without connecting the speaker.

LC Filter constants

RL	L1	C1
4Ω	10μH	1.0μF
8Ω	22μH	0.47μF
16Ω	47μH	0.22μF



LC Filter circuit

●Control Function

Sleep Function

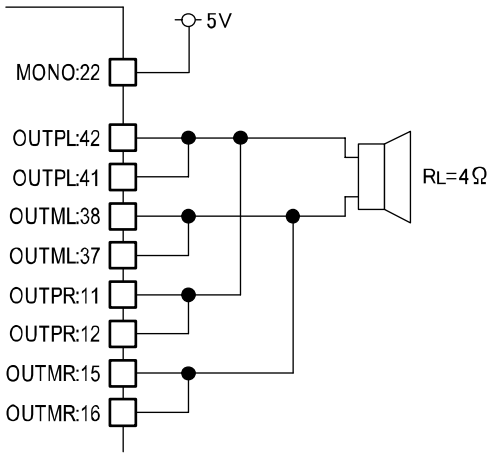
When SLEEPN terminal is “L”, YDA142 enters Sleep Mode.
The mode stops all the circuit functions including 5V Regulator and minimizes consumption current. At this time, the output stage of the digital amplifier is disabled and LINEOUTL and LINEOUTR terminals get undefined. And, PROTN terminal becomes “High-Z”.

Mute Function

When MUTEN terminal is “L”, YDA142 enters Mute Mode.
In this mode, the output stage of the digital amplifier is disabled and LINEOUTL and LINEOUTR terminals output audio signals normally.

Monaural Function

When MONO terminal is "H", YDA142 enters Monaural Mode.
In this mode, L channel input signal is output.
The mode can output up to 19W power into a 4Ω load resistor by short-circuiting between OUTPL and OUTPR terminals and between OUTML and OUTMR terminals.
In addition, LINEOUTL terminal outputs L channel input signals but LINEOUTR terminal gets undefined.
Switch between Monaural Mode and Stereo Mode during SLEEP Mode or a power shutdown state.



Output terminal connection when monaural mode

●Protection Function

YDA142 has the following protection functions: Over-current Protection function, Thermal Protection function, Clock Stop Protection function, Under-voltage Malfunction Prevention function, and DC Input Detection function.

Over-current Protection Function

This is a function to make the Over-current Protection Mode (disables the output stage of a digital amplifier in conjunction with "L" output to PROTN terminal) by detecting a short-circuiting (Ground short/Power supply short/Short between terminals) in the output stage of a digital amplifier.
This mode can be cancelled by power supply shutdown or SLEEPN terminal "L" setting.
In addition, the mode can be automatically resumed after the over-current detection by connecting PROTN terminal to SLEEPN terminal.

Thermal Protection Function

This is a function to make the Thermal Protection Mode (disables the output stage of a digital amplifier in conjunction with "L" output to PROTN terminal) by detecting extraordinary high temperature on YDA142. This mode can be cancelled by sufficient temperature decrease, power supply shutdown, or SLEEPN terminal "L" setting.
In addition, the mode can be automatically resumed after the high temperature detection by connecting PROTN terminal to SLEEPN terminal.

Clock Stop Protection Function

This is a function to make the Clock Stop Protection Function (disables the output stage of a digital amplifier) when a SCLK signal frequency of the digital interface becomes a frequency lower than Stop Detection Frequency (F_{UFP}).
The mode can be cancelled by returning the carrier clock frequency to the normal value.

Under-voltage Malfunction Prevention Function

This is a function to make the Under Voltage Protection Function (disables the output stage of a digital amplifier in conjunction with setting "High-Z" state to PROTN terminal) when a voltage at 12V power supply terminal (PVDDREG) becomes lower than the Under Voltage Detection Threshold Voltage (V_{UVPL}) or a voltage at 5V power supply terminal (DVDD) becomes lower than the Under Voltage Detection Threshold Voltage (V_{UVAL}).
The built-in 5V regulator is also disabled when a voltage at 12V power supply terminal becomes lower than the Threshold Voltage V_{UVPL}.
The mode can be cancelled when "L" is set to SLEEPN terminal or a voltage of each power supply terminal becomes higher than the Threshold Voltage (V_{UVPH}, V_{UVAH}).

DC Input Detection Function

This is a function to make the DC Input Protection Mode (disables digital amplifier output stage) when a digital input signal of the DC input detection voltage level (V_{DCIN}) or more continues over the DC input detection time (T_{DCIN}) without change of polarity.
DC Input Protection Mode is cancelled when "L" is set to SLEEPN terminal or a digital input signal becomes lower than V_{DCIN} or its polarity is changed.

●5V Regulator Function

YDA142 outputs 5V (V_{REG}) to REFA terminal when SLEEPN terminal is "H". Connect a capacitor of 0.1μF or over to REFA terminal for stabilization.
Connect the REFA terminal to DVDD terminal on a board.
And, don't connect the REFA terminal to other terminals except DVDD terminal and YDA142 input terminals.

●Pop-noise Reduction Function

Pop-noise Reduction Function works when powered on, when shut down, when SLEEP ON/OFF is switched, or when Mute ON/OFF is switched.

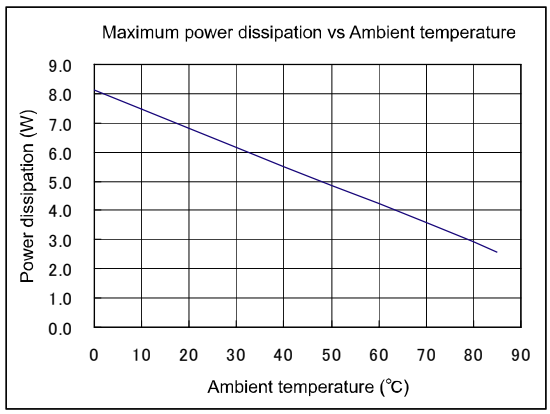
●Power dissipation

The power dissipation of YDA142 is limited by junction temperature rating (125℃) and package thermal resistance (15.4℃/W: 4-layer board).
The power dissipation and junction temperature can be found by the following formula.
When used, take care so that the power dissipation and junction temperature do not exceed the absolute maximum ratings.

・Formula for the power dissipation

$$Ploss = (Pout \times Rpn / Rl) \times 2 + Idc \times Vdc$$

Ploss	: Power Dissipation (W)
Pout	: Output Power (W)
Rpn	: 0.66 (constant)
Rl	: Load Resistance (Ω)
Idc	: 0.035(constant/at V_{DDP}=12V) 0.028(constant/at V_{DDP}=9V) 0.038(constant/at V_{DDP}=13.5V)
Vdc	: Supply Voltage (V)



Maximum Power Dissipation

・Formula for the junction temperature

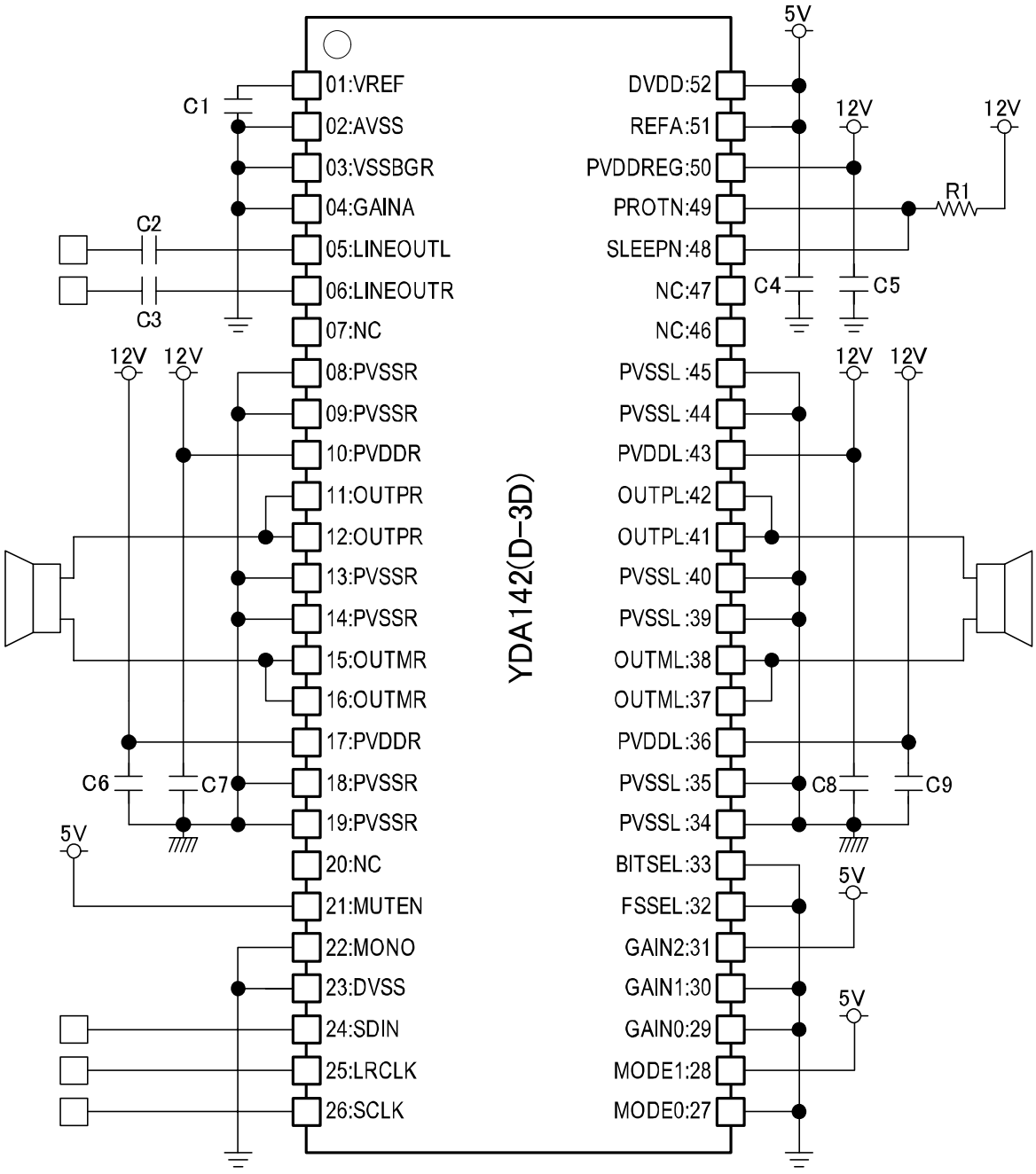
$$Tj = Ploss \times \theta ja + Ta$$

Ploss	: Power Dissipation (W)
θja	: 15.4(constant/package thermal resistance (℃/W), 4-layer board)
Ta	: Ambient temperature (℃)

●Package thermal resistance

The package (52SSOP) for YDA142 has a Thermal Pad for radiation on the surface. Use this Thermal Pad by soldering on a board.
The package's thermal resistance is 15.4℃/W (4-layer board). This thermal resistance is a value measured under the following conditions: board size 136mm×85mm, 1st layer and 4th layer copper foil board density 154%, 2nd layer and 3rd layer copper foil board density 200%, no wind. In addition, the lower side pattern of the Thermal Pad is connected to all the layers in a board by through holes (φ0.4).

■Example of application circuit



ID	Value	Element
C1	1μF/16V	Multilayer ceramic capacitor
C2,C3	1μF/16V	Multilayer ceramic capacitor
C4	0.1μF/16V	Multilayer ceramic capacitor
C5	1μF/25V	Multilayer ceramic capacitor
C6,C7,C8,C9	4.7μF/25V	Multilayer ceramic capacitor
R1	100kΩ, 1/16W	Chip Resistor

■Electrical characteristics

●Absolute Maximum Ratings Note 6)

Item	Symbol	Min.	Max.	Unit
Power Supply Terminal (VDDP) voltage range Note 1,2,3)	V_{DDP}	-0.3	14.0	V
SLEEPN, PROTN terminal voltage range	V_{IN1}	V_{SS}-0.3	V_{DDP}+0.3	V
Control line terminal voltage range Note 4)	V_{IN3}	V_{SS}-0.3	V_{REG}+0.3	V
Input/Output terminal voltage range Note 5)	V_{IN4}	V_{SS}-0.3	V_{REG}+0.3	V
Power Dissipation (Ta=25℃, 4-layer board)	P_{D25}		6.4	W
Power Dissipation (Ta=70℃, 4-layer board)	P_{D70}		3.6	W
Junction Temperature	T_{JMAX}		125	℃
Storage Temperature	T_{STG}	-50	125	℃

Note 1) VSS means AVSS, VSSBGR, DVSS, PVSSR, and PVSSL. Keep all the VSS terminals at the same potential.

Note 2) The voltage is based on V_{SS}=0V.

Note 3) The power supply terminal (VDDP) means PVDDREG, PVDDR, and PVDDL terminal.

Note 4) The control input/output terminal means MUTEN, MONO, GAIN[2:0], MODE[1:0], BITSEL, FSSEL, SCLK, LRCLK, and SDIN terminal.

Note 5) The input/output terminal means VREF and GAINA terminal.

Note 6) Absolute Maximum Ratings is values which must not be exceeded to guarantee device reliability and life, and when using a device in excess even a moment, it may immediately cause damage to device or may significantly deteriorate its reliability.

●Recommended operating condition

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage Note 7)	V_{DDP}	9.0	12.0	13.5	V
Operating Ambient Temperature	T_a	-40	25	85	℃
Speaker Impedance (Stereo)	R_{LS}	7.5	8		Ω
Speaker Impedance (Mono)	R_{LM}	3.75	4		Ω

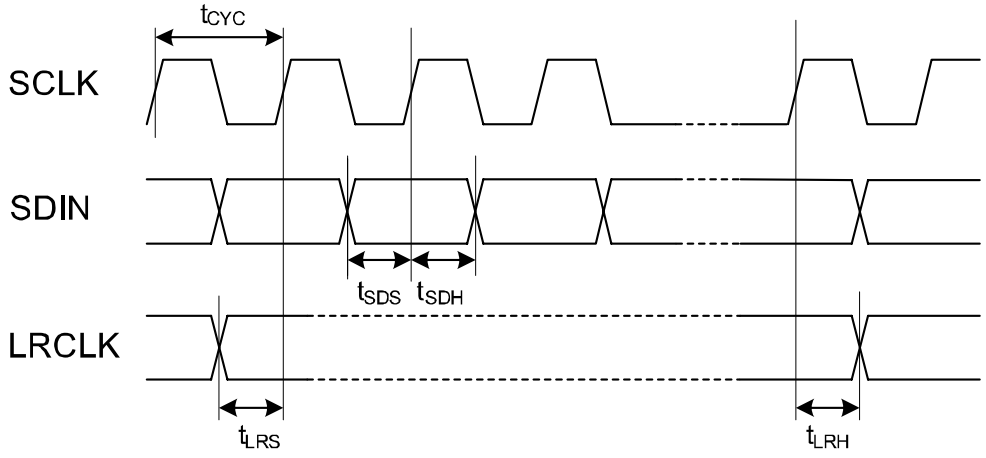
Note 7) All the voltages are based on V_{SS}=0V.

●DC Characteristics (V_{SS}=0V, V_{DDP}=12V±0.5V, Ta=0℃ to 85℃, unless otherwise specified)

Item	Symbol	Min.	Typ.	Max.	Unit
REFA output terminal voltage	V_{REG}	4.5	5	5.5	V
DVDD input terminal voltage	V_{DVDD}	4.5	5	5.5	V
PROTN terminal Low level output voltage (I_{OL}=1.6mA)	V_{OLP}			0.4	V
SLEEPN terminal High level input voltage	V_{IH1}	2.2			V
SLEEPN terminal Low level input voltage	V_{IL1}			0.8	V
Control line input terminal High Level input voltage	V_{IH2}	2.2			V
Control line input terminal Low Level input voltage	V_{IL2}			0.8	V
PVDDREG terminal Startup threshold voltage	V_{UVPH}		8.0		V
PVDDREG terminal Shut-down threshold voltage	V_{UVPL}		7.6		V
DVDD terminal Startup threshold voltage	V_{UVAH}		3.7		V
DVDD terminal Shut-down threshold voltage	V_{UVAL}		3.3		V
DC input detection voltage level	V_{DCIN}		18		dBFS
Consumption current (SLEEP Mode)	I_{SLEEP}		1		μA
Consumption current (Mute Mode)	I_{MUTE}		20		mA
Consumption current (Silent, without filter)	I_{DDD}		40		mA

●AC Characteristic (V_{SS}=0V, V_{DDP}=12V±0.5V, Ta=0℃ to 85℃, unless otherwise specified)

Item	Symbol	Min.	Typ.	Max.	Unit
Carrier Clock Frequency (Fs=44.1kHz)	F_{CK}		470		kHz
Carrier Clock Frequency (Fs=48kHz, 32kHz)	F_{CK}		500		kHz
Clock stop detection SCLK signal frequency	F_{UFP}		400		kHz
DC input detection time	T_{DCIN}	1.8	2	3.7	s
SCLK cycle time	T_{CYC}	250		600	ns
LRCLK setup time	T_{LRS}	60			ns
LRCLK hold time	T_{LRH}	25			ns
SDIN setup time	T_{SDS}	60			ns
SDIN hold time	T_{SDH}	25			ns



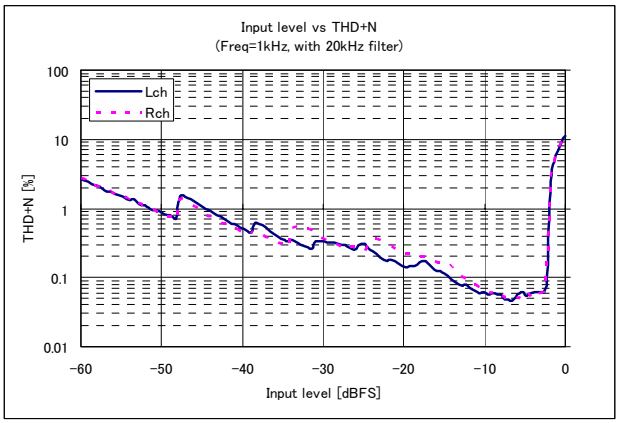
●Analog Characteristics (V_{SS}=0V, V_{DDP}=12V, Ta=25℃, Frequency:1kHz, unless otherwise specified)

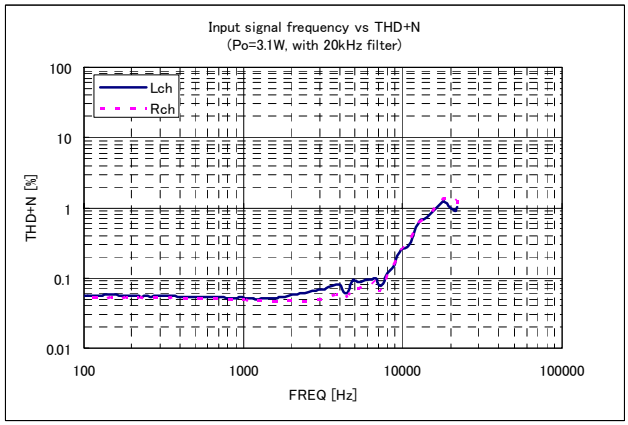
Item	Conditions	Symbol	Min.	Typ.	Max.	Unit
Maximum output (Stereo) (THD+N=10%)	R_L=8Ω	P_O		9.5		W
Maximum output (Mono) (THD+N=10%)	R_L=4Ω			19.0		W
Voltage Gain (GAIN[2:0]=H,L,L)		A_V		20		dB
Total Harmonic Distortion Rate (Stereo) (BW: 20kHz)	R_L=8Ω, P_O=5W	THD+N		0.05		%
Total Harmonic Distortion Rate (Mono) (BW: 20kHz)	R_L=4Ω, P_O=9.5W			0.1		%
Signal /Noise Ratio (BW: 20kHz A-Filter)	R_L=8Ω, P_O=9.5W, GAIN[2:0]=H,L,L	SNR		100		dB
Channel Separation Ratio		CS		-78		dB
Maximum Efficiency	R_L=8Ω, P_O=9.5W	η		90		%
Output offset voltage		V_O		±20		mV

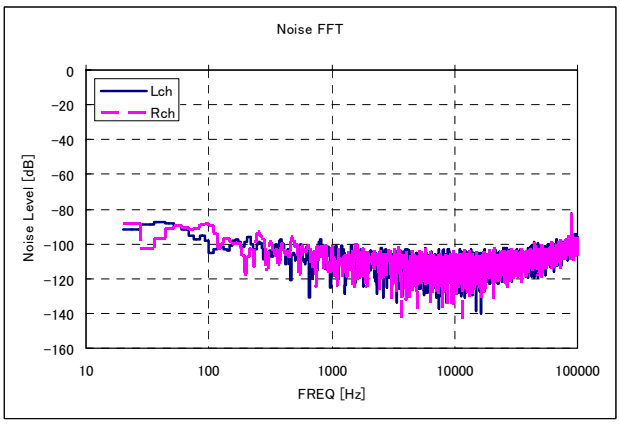
Note) All the values of analog characteristics were obtained by using our evaluation circumstance.
Depending upon parts and pattern layout to use, characteristics may be changed.
8Ω resistor and 30μH coil are used as an output load in order to obtain various digital amplifier characteristics.

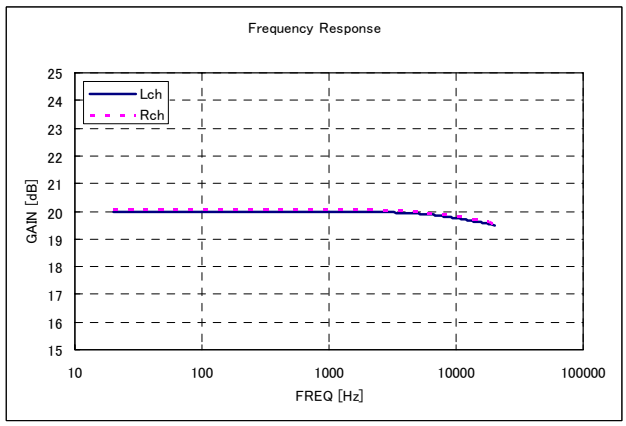
■Typical characteristics examples

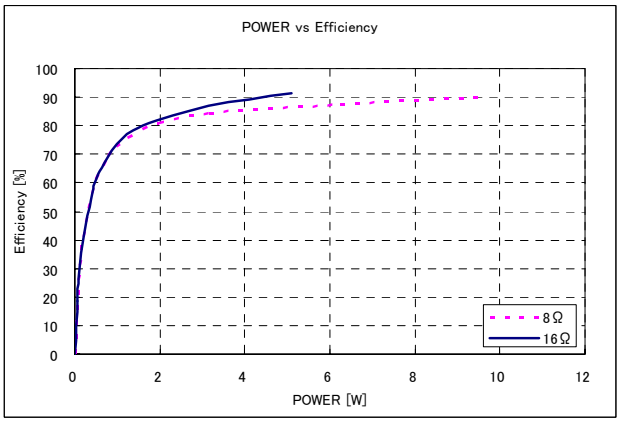
●Digital Amplifier Characteristics (V_{DDP}=12V, Ta=25℃, R_L=8Ω+30μH, Frequency=1kHz)

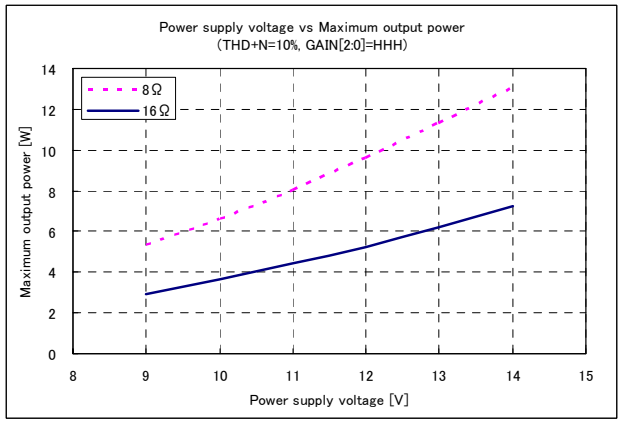


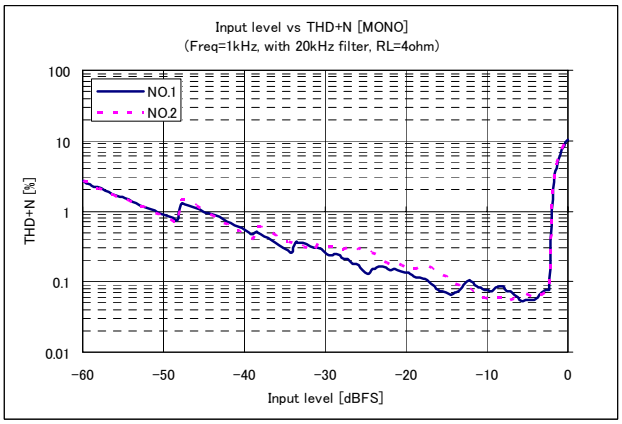


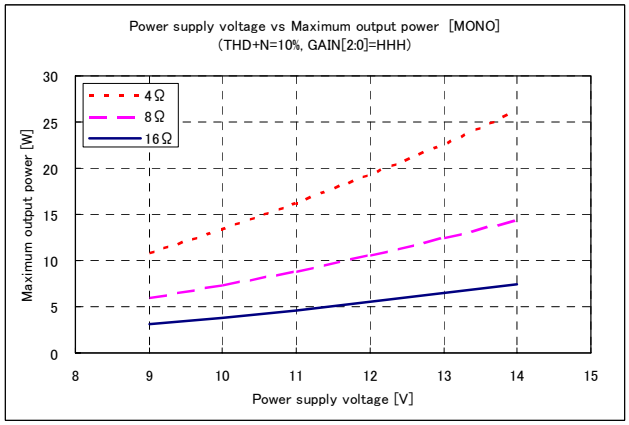






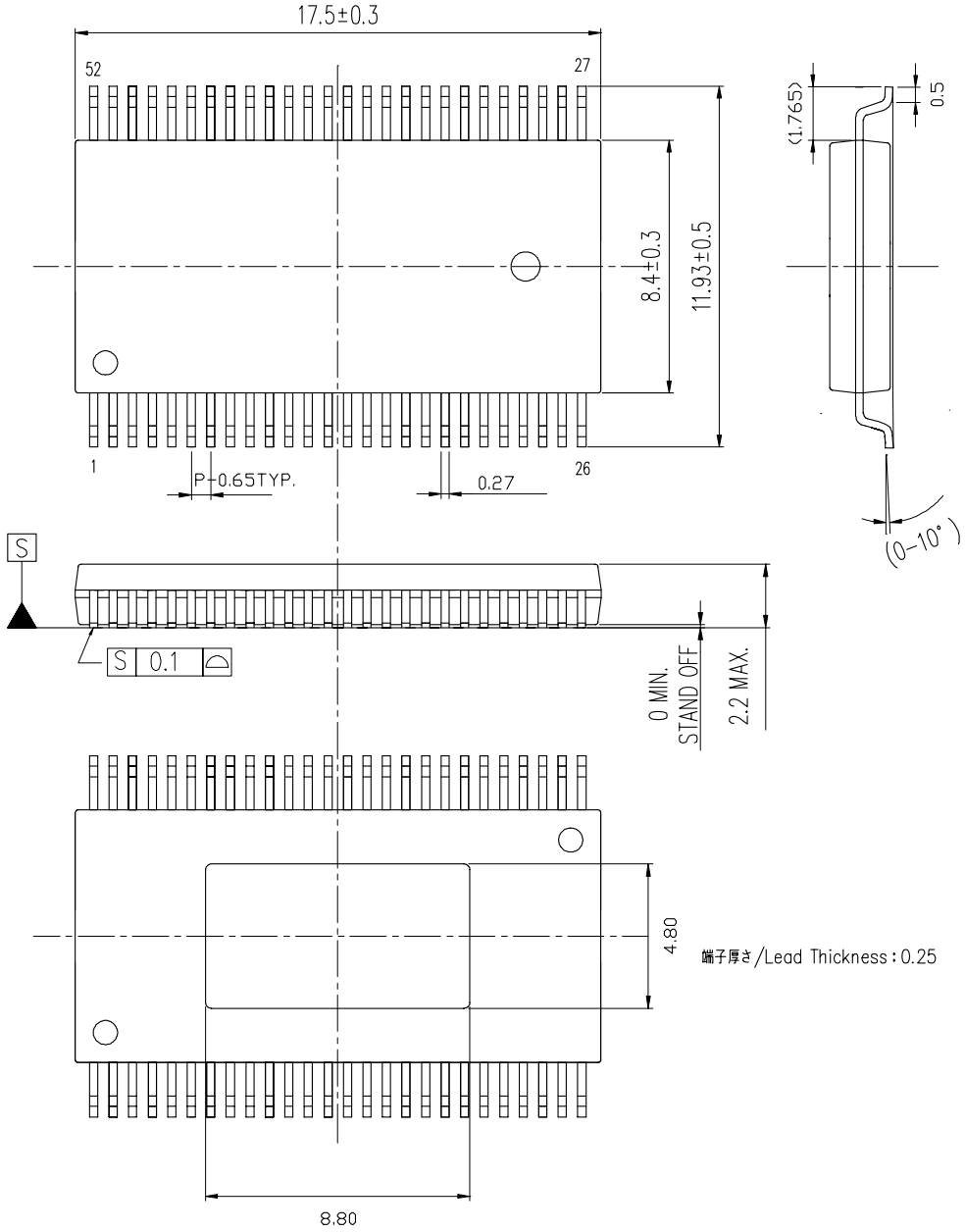






■Package outline

C-PK52EP-1



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位： mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
For detailed information, please contact your local Yamaha agent.

MEMO

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