Z80181

SMART ACCESS CONTROLLER (SAC™)

FEATURES

- Z80180 Compatible MPU Core with 1 Channel of Z85C30 SCC, Z80 CTC, Two 8-Bit General-Purpose Parallel Ports, and Two Chip Select Signals.
- High Speed Operation (10 MHz)
- Low Power Consumption in Two Operating Modes:
  - (TBD) mA Typ. (Run Mode)
  - (TBD) mA Typ. (STOP Mode)
- Wide Operational Voltage Range (5V ±10%)
- TTL/CMOS Compatible
- Clock Generator
- One Channel of Z85C30 Serial Communication Controller (SCC)
- Z180 Compatible MPU Core Includes:
  - Enhanced Z80 CPU Core
  - Memory Management Unit (MMU) Enables Access to 1MB of Memory
  - Two Asynchronous Channels
  - Two DMA Channels
  - Two 16-Bit Timers
  - Clocked Serial I/O Port
- On-Board Z84C30 CTC
- Two 8-Bit General-Purpose Parallel Ports
- Memory Configurable RAM and ROM Chip Select Pins
- 100-Pin QFP Package

GENERAL DESCRIPTION

The Z80181 SAC™ Smart Access Controller (hereinafter, referred to as Z181 SAC) is a sophisticated 8-bit CMOS microprocessor that combines a Z180-compatible MPU (Z181 MPU), one channel of Z85C30 Serial Communication Controller (SCC), a Z80 CTC, two 8-bit general-purpose parallel ports, and two chip select signals, into a single 100-pin Quad Flat Pack (QFP) package (Figures 1 and 2). Created using Zilog's patented Superintegration™ methodology of combining proprietary IC cores and cells, this high-end intelligent peripheral controller is well-suited for a broad range of intelligent communication control applications such as terminals, printers, modems, and slave communication processors for 8-, 16- and 32- bit MPU based systems.

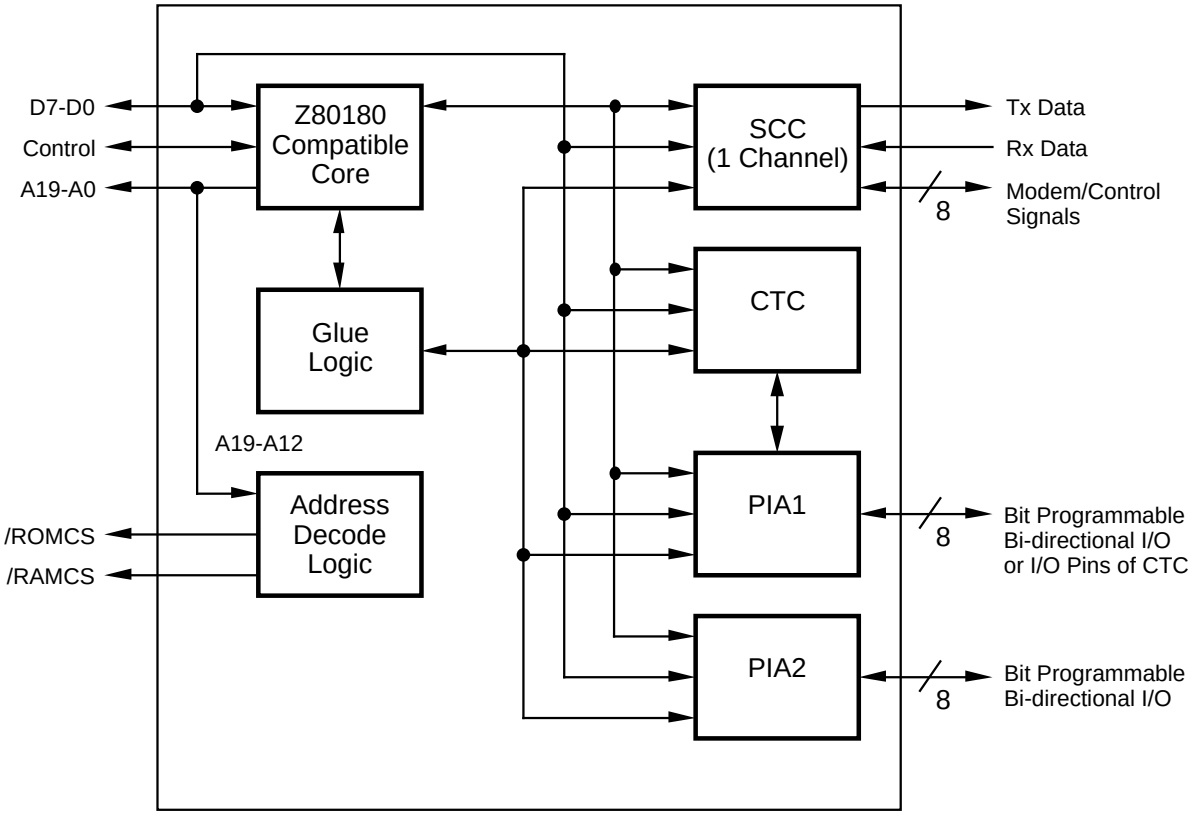
Information on enhancement/cost reductions of existing hardware using Z80/Z180 with Z8530/Z85C30 applications is also included in this product specification.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Z80181 = Z180 + SCC/2 + CTC + PIA

Figure 1. Z80181 Functional Block Diagram

PIN DESCRIPTION

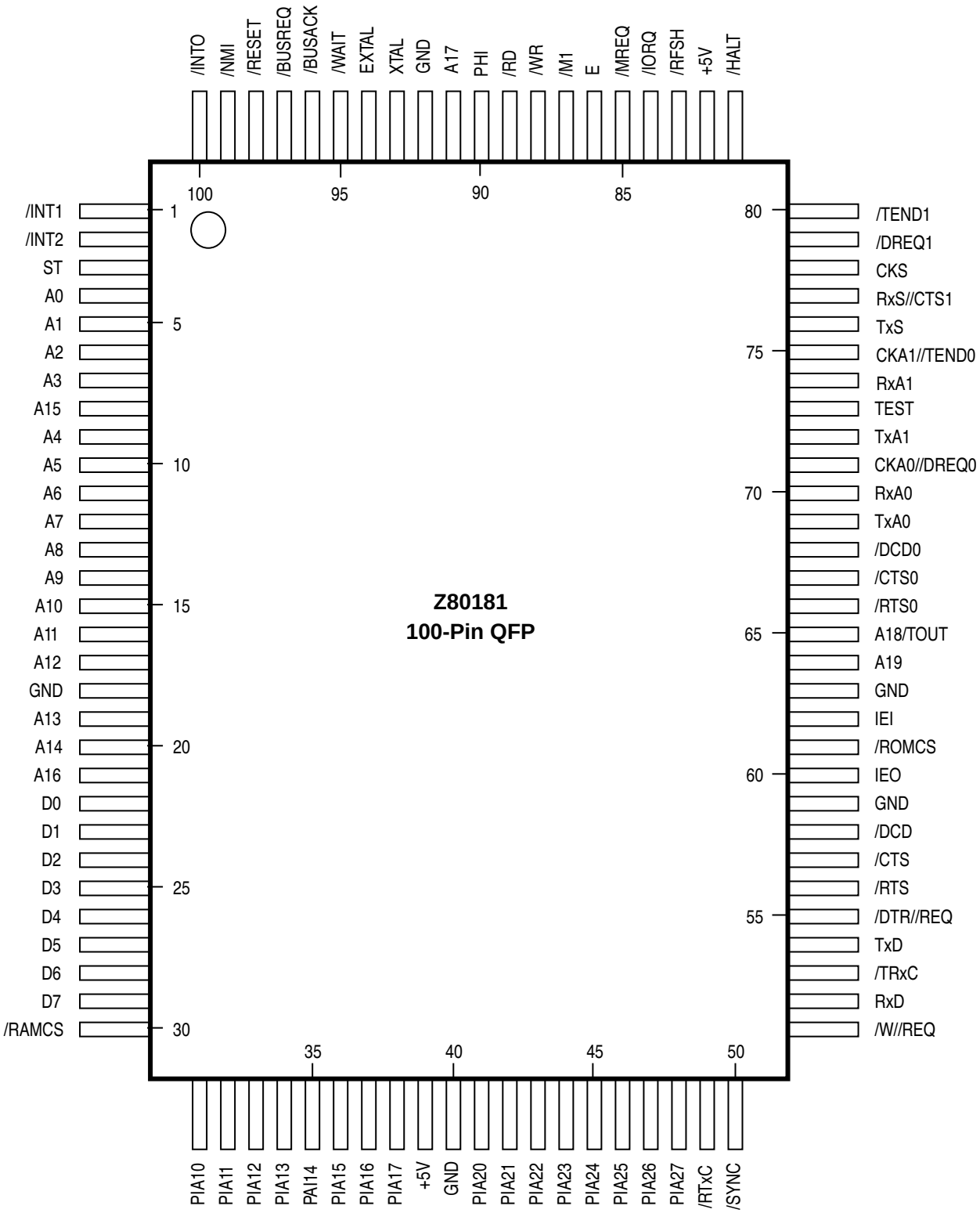


Figure 2. 100-Pin QFP Pin Configuration

CPU SIGNALS

Pin Name	Pin Number	Input/Output, Tri-State	Function
A19 - A0	4-17, 19-21, 64, 65, 91	I/O, Active 1	**Address Bus.** A19 - A0 form a 20-bit address bus which specifies I/O and memory addresses to be accessed. During the refresh period, addresses for refreshing are output. The address bus enters a high-impedance state during Reset and external bus acknowledge cycles. The bus is an input when the external bus master is accessing the on-chip peripherals. Address line A18 is multiplexed with the output of PRT Channel 1 (T_{OUT}, selected as address output on Reset).
D0-D7	22-29	I/O, Active 1	**8-Bit Bidirectional Data Bus.** When the on-chip CPU is accessing on-chip peripherals, these lines are outputs and hold the data to/from the on-chip peripherals.
/RD	89	I/O, Active 0	**Read Signal.** CPU read signal for accepting data from memory or I/O devices. When an external master is accessing the on-chip peripherals, it is an input signal.
/WR	88	I/O, Active 0	**Write Signal.** This signal is active when data to be stored in a specified memory or peripheral device is on the MPU data bus. When an external master is accessing the on-chip peripherals, it is an input signal.
/MREQ	85	I/O, tri-state, Active 0	**Memory Request Signal.** When an effective address for memory access is on the address bus, /MREQ is active. This signal is analogous to the /ME signal of the Z64180.
/IORQ	84	I/O, tri-state, Active 0	**I/O Request Signal.** When addresses for I/O are on the lower 8 bits (A7-A0) of the address bus in the I/O operation, "0" is output. In addition, the /IORQ signal is output with the /M1 signal during the interrupt acknowledge cycle to inform peripheral devices that the interrupt response vector is on the data bus. This signal is analogous to the /IOE signal of the Z64180.
/M1	87	I/O, tri-state, Active 0	**Machine Cycle "1".** /MREQ and /M1 are active together during the operation code fetch cycle. /M1 is output for every opcode fetch when a two byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with /IORQ. It is also used with /HALT and ST signal to decode the status of the CPU Machine cycle. This signal is analogous to the /LIR signal of the Z64180.
/RFSH	83	Out, tri-state, Active 0	**The Refresh Signal.** When the dynamic memory refresh address is on the low order 8-bits of the address bus (A7 - A0), /RFSH is active along with the /MREQ signal. This signal is analogous to the /REF signal of the Z64180.

Pin Name	Pin Number	Input/Output, Tri-State	Function
/INT0	100	Wired-OR I/O, Active 0	**Maskable Interrupt Request 0.** Interrupt is generated by peripheral devices. This signal is accepted if the interrupt enable Flip-Flop (IFF) is set to "1". Internally, the SCC and CTC's interrupt signals are connected to this line, and require an external pull-up resistor.
/INT1, /INT2	1, 2,	In, Active 0	**Maskable Interrupt Request 1 and 2.** This signal is generated by external peripheral devices. The CPU honors these requests at the end of current instruction cycle as long as the /NMI, /BUSREQ and /INT0 signals are inactive. The CPU will acknowledge these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgment for /INT0, during this cycle, neither /M1 or /IORQ will become active.
/NMI	99	In, Active 0	**Non-Maskable Interrupt Request Signal.** This interrupt request has a higher priority than the maskable interrupt request and does not rely upon the state of the interrupt enable Flip-Flop (IFF).
/HALT	81	Out, tri-state, Active 0	**Halt Signal.** This signal is asserted after the CPU has executed either the HALT or SLP instruction, and is waiting for either non-maskable interrupt maskable interrupt before operation can resume. It is also used with the /M1 and ST signals to decode the status of the CPU machine cycle.
/BUSREQ	97	In, Active 0	**BUS Request Signal.** This signal is used by external devices (such as a DMA controller) to request access to the system bus. This request has higher priority than /NMI and is always recognized at the end of the current machine cycle. This signal will stop the CPU from executing further instructions and place the address bus, data bus, /MREQ, /IORQ, /RD and /WR signals into the high impedance state. /BUSREQ is normally wired-OR and a pull-up resistor is externally connected.
/BUSACK	96	Out, Active 0	**Bus Acknowledge Signal.** In response to /BUSREQ signal, /BUSACK informs a peripheral device that the address bus, data bus, /MREQ, /IORQ, /RD and /WR signals have been placed in the high impedance state.
/WAIT	95	Wired-OR I/O, Active 0	**Wait Signal.** /WAIT informs the CPU that the specified memory or peripheral is not ready for a data transfer. As long as /WAIT signal is active, the MPU is continuously kept in the wait state. Internally, the /WAIT signal from the SCC interface logic is connected to this line, and requires an external pull-up resistor.

PERIPHERAL SIGNALS

Pin Name	Pin Number	Input/Output, Tri-State	Function
RXA0, RXA1	70, 74	In, Active 1	**ASCI Receive Data 0 and 1.** These signals are the receive data to the ASCI channels.
TXA0, TXA1	69, 72	Out, Active 1	**ASCI Transmit Data 0 and 1.** These signals are the receive data to the ASCI channels. Transmit data changes are with respect to the falling edge of the transmit clock.
/RTS0	66	Out, Active 0	**Request to Send 0.** This is a programmable modem control signal for ASCI channel 0.
/DCD0	68	In, Active 0	**Data Carrier Detect 0.** This is a programmable modem control signal for ASCI channel 0.
/CTS0	67	In, Active 0	**Clear To Send 0.** This is a programmable modem control signal for ASCI channel 0.
/CTS1/RXS	77	In, Active 0	**Clear To Send 0/Clocked Serial Receive Data.** This is a programmable modem control signal for ASCI channel 0. Also, this signal becomes receive data for the CSIO channel under program control. On power-on Reset, this pin is set as RxS.
CKA0//DREQ0	71	I/O, Active 1	**Asynchronous Clock0/DMAC0 Request.** This pin is the transmit and receive clock for the Asynchronous channel 0. Also, under program control, this pin is used to request a DMA transfer from DMA channel 0. DMA0 monitors this input to determine when an external device is ready for a read or write operation. On power-on Reset, this pin is initialized as CKA0.
CKA1//TEND0	75	I/O, Active 1	**Asynchronous Clock1/DMAC0 Transfer End.** This pin is the transmit and receive clock for the Asynchronous channel 1. Also, under program control, this pin becomes /TEND0 and is asserted during the last write cycle of the DMA0 operation and is used to indicate the end of the block transfer. On power-on Reset, this pin initializes as CKA1.
/TEND1	80	Out, Active 0	**DMAC1 Transfer End.** This pin is asserted during the last write cycle of the DMA1 operation and is used to indicate the end of the block transfer.
CKS	78	I/O, Active 1	**CSIO Clock.** This line is the clock for the CSIO channel.
TXS	76	Out, Active 1	**CSI/O Tx Data.** This line carries the transmit data from the CSIO channel.
/DREQ1	79	In, Active 0	**DMAC1 Request.** This pin is used to request a DMA transfer from DMA channel 1. DMA1 monitors this input to determine when an external device is ready for a read or write operation.

SCC SIGNALS

Pin Name	Pin Number	Input/Output, Tri-State	Function
/W//REQ	51	Active 0	**Wait/Request.** Open-drain when programmed for a Wait function, driven "1" or "0" when programming for a Request function. Used as /WAIT or /REQUEST depending upon SCC programming. When programmed as /WAIT, this signal is asserted to alert the CPU that addressed memory or I/O devices are not ready and that the CPU should wait. When programmed as /REQUEST, this signal is asserted when a peripheral device associated with a DMA port is ready to read/write data. After reset, this pin becomes "/WAIT".
/SYNC	50	I/O, Active 0	**Synchronization.** This pin can act either as input, output, or part of the crystal oscillator circuit. In asynchronous receive mode (crystal oscillator option not selected), this pin is an input similar to /CTS and /DCD. In this mode, transitions on this line affect the state of the Sync/Hunt status bit in Read Register 0 but has no other function.
			In external sync mode with crystal oscillator option not selected, this line also acts as an input. In this mode, /SYNC must be driven "0" two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of /SYNC.
			In internal sync mode (Monosync and Bisync) with the crystal oscillator option not selected, this line acts as output and is active only during the part of the receive clock cycle in which a synchronous character is recognized (regardless of character boundaries). In SDLC mode, this pin acts as an output and is valid on receipt of a flag.
RxD	52	In, Active 1	**Receive Data.** This input signal receives serial data at standard TTL levels.
/RTxC	49	In, Active 0	**Receive/Transmit Clock.** This pin can be programmed in several different modes of operation. /RTxC may supply the receive clock, the transmit clock, the clock for the Baud Rate Generator, or the clock for the Digital Phase-Locked Loop. This pin can also be programmed for use with the /SYNC pin as a crystal oscillator. The receive clocks can be 1, 16, 32, or 64 times the data transfer rate in Asynchronous mode.
/TRxC	53	I/O, Active 0	**Transmit/Receive Clock.** This pin can be programmed in several different modes of operation. /TRxC can supply the receive clock or the transmit clock in the input mode. Also, it can supply the output of the Digital Phase-Locked Loop, the crystal oscillator, the Baud Rate Generator, or the transmit clock in the output mode.

SCC SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, Tri-State	Function
TxD	54	Out, Active 1	**Transmit Data.** This Output signal transmits serial data at standard TTL level.
/DTR//REQ	55	Out, Active 0	**Data Terminal Ready/Request.** This output follows the state programmed into the DTR bit. It can also be used as general-purpose output or as Request line for a DMA controller.
/RTS	56	Out, Active 0	**Request To Send.** When the RTS bit in Write Register 5 is set, the /RTS signal goes low. When the RTS bit is reset in Asynchronous mode and auto enable is on, the signal goes high after the transmitter is empty. In synchronous mode or in Asynchronous mode, with Auto Enable off, the /RTS pin follows the state of the RTS bit. This pin can be used as a general-purpose output.
/CTS	57	In, Active 0	**Clear To Send.** If this pin is programmed as auto enable, a "0" on the input enables the transmitter. If not programmed as Auto Enable, it may be used as a general-purpose input. This input is Schmitt-trigger buffered to accommodate inputs with slow rise times. The SCC detects pulses on this input and can interrupt the CPU on both logic level transitions.
/DCD	58	In, Active 0	**Data Carrier Detect.** This pin functions as receiver enable if it is programmed for auto enable. Otherwise, it may be used as a general-purpose input. This input is Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on this input and can interrupt the CPU on both logic level transitions.

PIA/CTC SIGNALS

Pin Name	Pin Number	Input/Output, Tri-State	Function
PIA17-PIA14	35-38	I/O	**Port 1 Data 7-Port 1 Data 4 or CTC ZC/TO3 - ZC/TO0.** These lines can be configured as inputs or outputs on a bit -by-bit basis. Also, under program control, these bits become Z80 CTC's ZC/TO3 - ZC/TO0, and in either timer or counter mode, pulses are output when the down counter has reached zero. On reset, these signals function as PIA17-14 and are inputs.
PIA13-PIA10	31-34	I/O	**Port 1 Data 3-Port 1 Data 0 or CTC CLK/TRG3-0.** These lines can be configured as inputs or outputs on a bit by bit basis. Also, under program control, these bits become Z80 CTC's CLK/TRG3-CLK/TRG0, and correspond to four Counter/Timer Channels. In the counter mode, each active edge causes the downcounter to decrement by one. In timer mode, an active edge starts the timer. It is program selectable whether the active edge is rising or falling. On reset, these signals are set to PIA13-10 as inputs.
PIA27-20	41-48	I/O	**Port 2 Data.** These lines are configured as inputs or outputs on a bit-by-bit basis. On reset, they are inputs.

SYSTEM CONTROL SIGNALS

Pin Name	Pin Number	Input/Output, Tri-State	Function
ST	3	Out, Active 1	**Status.** This signal is used with the /M1 and /HALT output to decode the status of the CPU machine cycle. Note that the /M1 output is affected by the status of the M1E bit in the OMCR register. The following table shows the status while M1E=1.

ST	/HALT	/M1	Operation
0	1	0	CPU Operation (1st Opcode fetch)
1	1	0	CPU Operation (2nd and 3rd Opcode fetch)
1	1	1	CPU Operation (MC other than Opcode fetch)
0	X	1	DMA operation
0	0	0	HALT mode
1	0	1	SLEEP mode (Incl. System STOP mode)

Pin Name	Pin Number	Input/Output, Tri-State	Function
IEI	62	In, Active 1	**Interrupt enable input signal.** IEI is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.
IEO	60	Out, Active 1	**The interrupt enable output signal.** In the daisy-chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is "1" and the CPU is not servicing an interrupt from the on-chip peripherals.
/ROMCS	61	Out, Active 0	**ROM Chip select.** Used to access ROM. Refer to "Functional Description" on chip select signals for further explanation.
/RAMCS	30	Out, Active 0	**RAM Chip Select.** Used to access RAM. Refer to "Functional Description" on chip select signals for further explanation.
/RESET	98	In, Active 0	**Reset signal.** /RESET signal is used for initializing the MPU and other devices in the system. It must be kept in the active state for a period of at least 3 system clock cycles.
EXTAL	94	In, Active 1	**Crystal oscillator connecting terminal.** A parallel resonant crystal is recommended. If an external clock source is used as the input to the Z180 Clock Oscillator unit, supply the clock into this terminal.
XTAL	93	Out	**Crystal oscillator connecting terminal.**
PHI	90	Out, Active 1	**System Clock.** Single-phase clock output from Z181 MPU.
E	86	Out, Active 1	**Enable Clock.** Synchronous Machine cycle clock output during a bus transaction.
TEST	73	Out	**Test pin.** Used in the open state.
V_{CC}	39, 82		**Power Supply.** +5 Volts
V_{SS}	18, 40, 59, 63, 92		**Power Supply.** 0 Volts

FUNCTIONAL DESCRIPTION

Functionally, the on-chip Z181 MPU, SCC, and CTC are the same as the discrete devices (Figure 1). Therefore, refer to the Product Specification/Technical Manual of each discrete product for a detailed description of each individual unit. The following subsections describe each individual functional unit of the SAC.

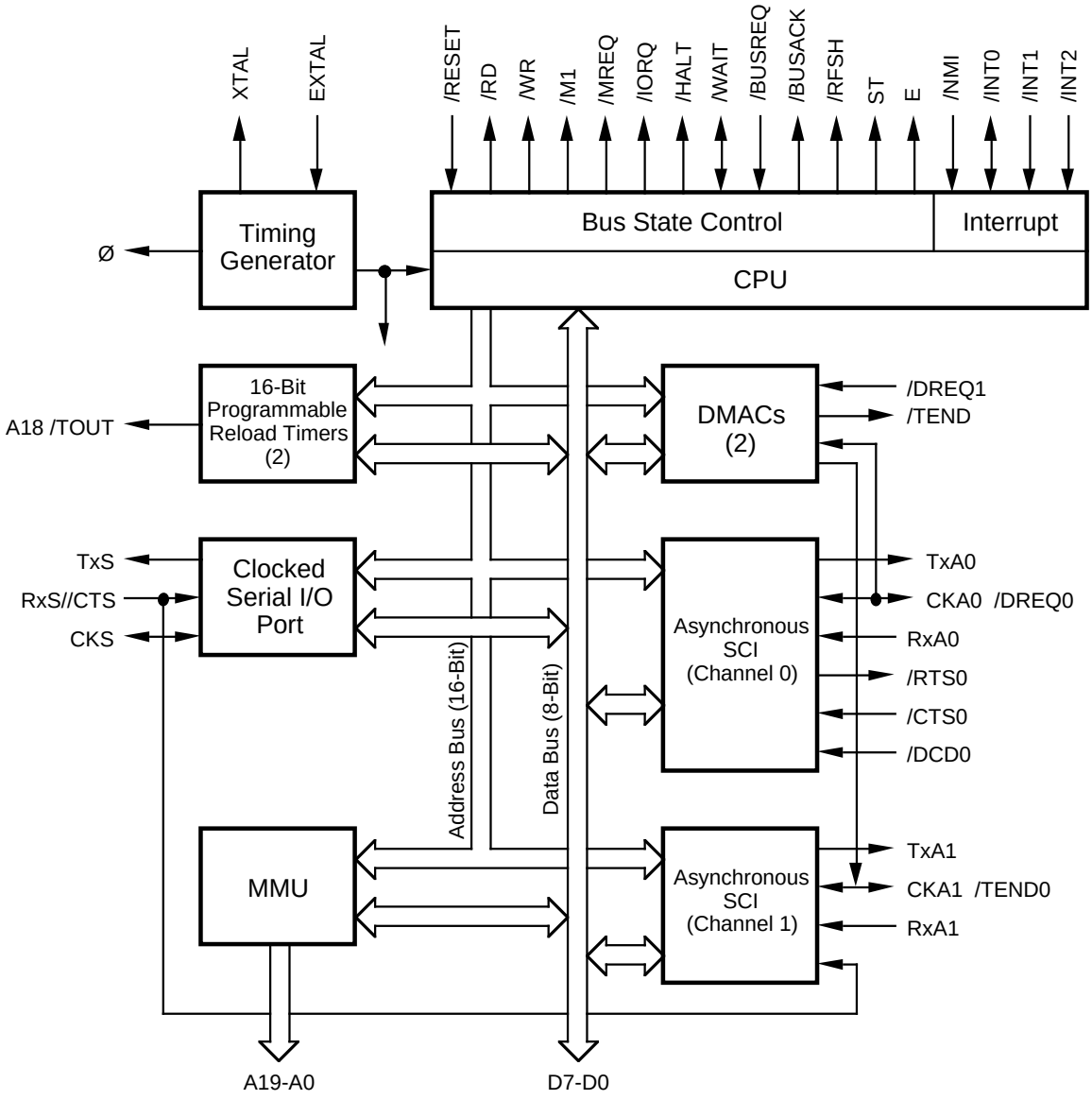


Figure 3. Z181 MPU Block Diagram

Z181 MPU

This unit provides all the capabilities and pins of the Zilog Z180 MPU. Figure 3 shows the Z181 MPU block diagram. This allows 100% software compatibility with existing Z180 (and Z80) software. Note that the on-chip I/O address should not be relocated to the I/O address (from 0C0h to 0FFh) to avoid address conflicts. The following is an overview of the major functional units of the Z181.

Z181 CPU

The Z181 CPU has 100% software compatibility with the Z80 CPU. In addition, the Z181 CPU has the following features:

Faster execution speed. The Z181 CPU is "fine tuned" making execution speed, on average, 10% to 20% faster than the Z80 CPU.

Enhanced DRAM Refresh Circuit. Z181 CPU's DRAM refresh circuit does periodic refresh and generates an 8-bit refresh address. It can be disabled or the refresh period adjusted, through software control.

Enhanced Instruction Set. The Z181 CPU has seven additional instructions to those of the Z80 CPU which include the MLT (Multiply) instruction.

HALT and Low Power Modes of Operation. The Z181 CPU has HALT and low power modes of operation, which are ideal for the applications requiring low power consumption like battery operated portable terminals.

System Stop Mode. When the Z181 SAC is in SYSTEM STOP mode, it is only the Z181 MPU which is in STOP mode. The on-chip CTC and SCC continue their normal operation.

Instruction Set. The instruction set of the Z181 CPU is identical to the Z180. For more details about each transaction, please refer to the Data Sheet/Technical Manual for the Z180/Z80 CPU.

Z181 CPU Basic Operation

Z181 CPU's basic operation consists of the following events. These are identical to the Z180 MPU. For more details about each operation, please refer to the Data Sheet/Technical manual for the Z180.

- Operation code fetch cycle
- Memory Read/Write operation
- Input/Output operation
- Bus request/acknowledge operation
- Maskable interrupt request operation
- Trap and Non-Maskable interrupt request operation
- HALT and low power modes of operation
- Reset Operation

Memory Management Unit (MMU)

The Memory Management Unit (MMU) allows the user to "map" the memory used by the CPU (64K bytes of logical addressing space) into 1M bytes of physical addressing space. The organization of the MMU allows object code compatibility with the Z80 CPU while offering access to an extended memory space. This is accomplished by using an effective "common area-banked area" scheme.

DMA Controller

The Z181 MPU has two DMA controllers. Each DMA controller provides high-speed data transfers between memory and I/O devices. Transfer operations supported are memory to memory, memory to/from I/O, and I/O to I/O. Transfer modes supported are request, burst, and cycle steal. The DMA can access the full 1M bytes addressing range with a block length up to 64K bytes and can cross over 64K boundaries.

Asynchronous Serial Communication Interface (ASCI)

This unit provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels also support a multiprocessor communication format.

Programmable Reload Timer (PRT)

The Z181 MPU has two separate Programmable Reload Timers, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is system clock divided by 20. PRT channel 1 provides an optional output to allow for waveform generation.

Clocked Serial I/O (CSI/O)

The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another CPU or MPU.

Programmable Wait State Generator

To ease interfacing with slow memory and I/O devices, the Z181 MPU unit has a programmable wait state generator. By programming the DMA/WAIT Control Register (DCNTL), up to three wait states are automatically inserted in memory and I/O cycles. This unit also inserts wait states during on-chip DMA transactions.

FUNCTIONAL DESCRIPTION (Continued)

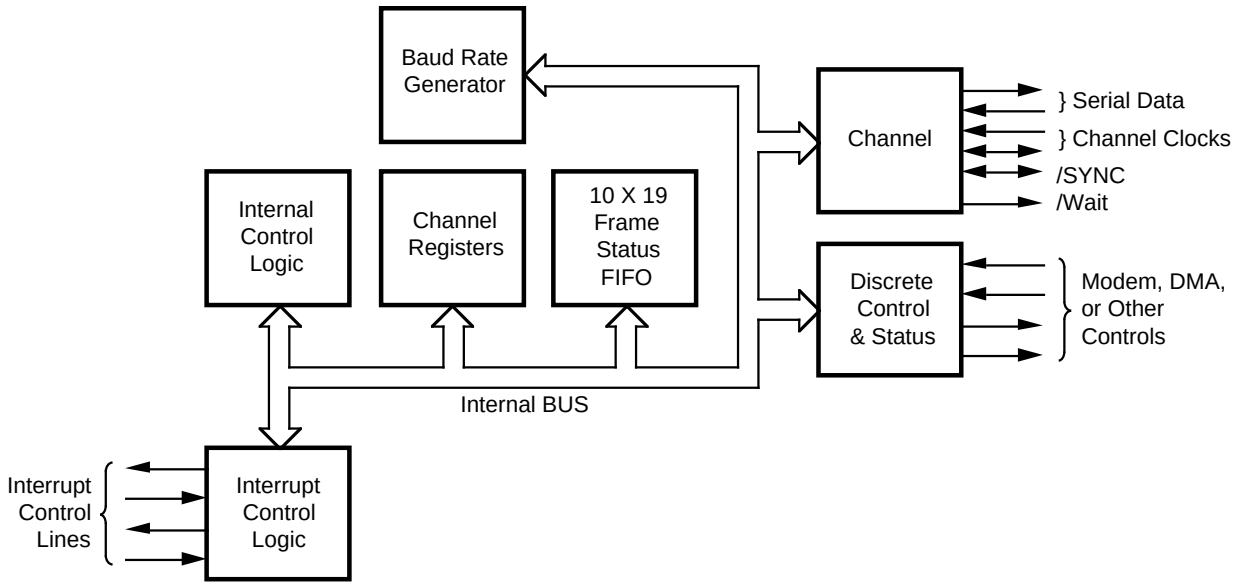


Figure 4. SCC Block Diagram

Z85C30 Serial Communication Controller Logic Unit

This logic unit provides the user with a multi-protocol serial I/O channel that is completely compatible with the two channel Z85C30 SCC with the following exceptions:

Their basic functions as serial-to-parallel and parallel-to-serial converters can be programmed by the CPU for a broad range of serial communications applications. This logic unit is capable of supporting all common asynchronous and synchronous protocols (Monosync, Bisync, and SDLC/HDLC, byte or bit oriented - Figure 4).

On the discrete version of the SCC (dual channel version), there are two registers shared between channels A and B, and two registers whose functions are different by channel. These are: WR2, WR9 (shared registers), and RR2 and RR3 (different functionality).

Following are the differences in functionality:

- **RR2** - Returns Unmodified Vector or modified vector depends on the status of "VIS" (Vector Include Status) bit in WR9.
- **RR3** - Returns IP status (Ch.A side).
- **WR9** - Ch.B Software Reset command has no effect.

The PCLK for the SCC is connected to PHI (System clock), the /INT signal is connected to /INT0 signal internally (requires external pull-up resistor) and SCC is reset when /RESET input becomes active. Interrupt from the SCC is handled through Mode 2 interrupt. During the interrupt acknowledge cycle, the on-chip SCC interface circuit inserts two wait states automatically.

Z84C30 Counter/Timer Logic Unit

This logic unit provides the user with four individual 8-bit Counter/Timer Channels that are compatible with the Z84C30 CTC (Figure 5). The Counter/Timers are programmed by the CPU for a broad range of counting and timing applications. Typical applications include event counting, interrupt and interval counting, and serial baud rate clock generation.

Each of the Counter/Timer Channels, designated Channels 0-3, have an 8-bit prescaler (when used in timer mode) and its own 8-bit counter to provide a wide range of count resolution. Each of the channels have their own Clock/Trigger input to quantify the counting process and an output to indicate zero crossing/timeout conditions. These signals are multiplexed with the Parallel Interface Adapter 1 (PIA1). With only one interrupt vector programmed into the logic unit, each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.

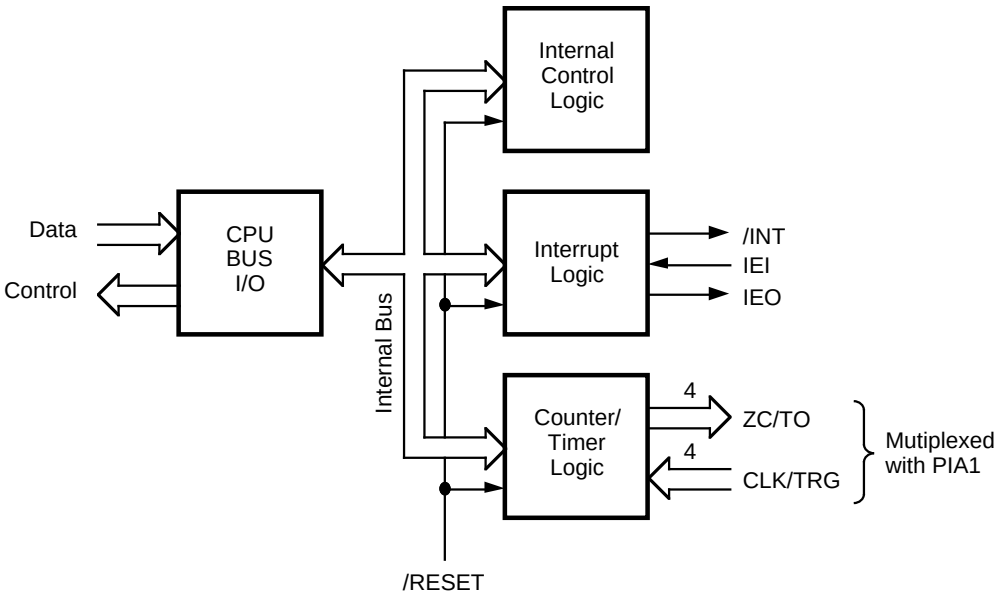


Figure 5. CTC Block Diagram

Parallel Interface Adapter (PIA)

The SAC has two 8-bit Parallel Interface Adapter (PIA) Ports. The ports are referred to as PIA1 and PIA2. Each port has two associated control registers; a Data Register and a register to determine each bit's direction (input or output). PIA1 is multiplexed with the CTC I/O pins. When the CTC I/O feature is selected, the CTC I/O functions override the PIA1 feature. Mode Selection is made through the System Configuration Register (Address: EDh; Bit D0). PIA1 has Schmitt-triggered inputs to have a better noise margin. These ports are inputs after reset.

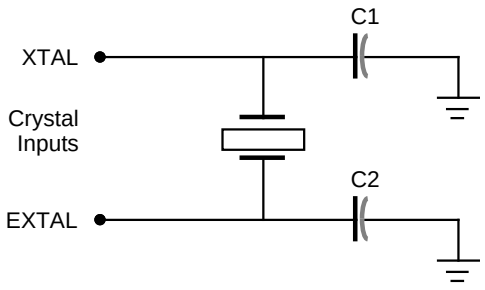


Figure 6. Circuit Configuration For Crystal

Clock Generator

The SAC uses the Z181 MPU's on-chip clock generator to supply system clock. The required clock is easily generated by connecting a crystal to the external terminals (XTAL, EXTAL). The clock output runs at half the crystal frequency. The system clock inputs of the SCC and the CTC are internally connected to the PHI output of the Z181 MPU.

FUNCTIONAL DESCRIPTION (Continued)

Recommended characteristics of the crystal and the values for the capacitor are as follows (the values will change with crystal frequency).

Type of crystal: Fundamental, parallel type crystal (AT cut is recommended).

Frequency tolerance: Application dependent.
CL, Load capacitance: Approximately 22 pF (acceptable range is 20-30 pF)

Rs, equivalent-series resistance: ≤ 30 Ohms
Drive level: 10 mW (for ≤ 10 MHz crystal) 5 mW (for ≥ 10 MHz crystal)

$C_{IN} = C_{OUT} = 15 \sim 22$ pF.

Chip Select Signals

The SAC has two chip select (/RAMCS, /ROMCS) pins. /ROMCS is the chip select signal for ROM and /RAMCS is the chip select signal for RAM. The boundary value for each chip select signal is 8 bits wide allowing all memory accesses with addresses less than or equal to this boundary value. This causes assertion of the corresponding /CS pin. These features are controlled through the RAM upper boundary address register (I/O address EAh), RAM lower boundary address register (I/O address EBh) and ROM upper boundary address register (I/O address ECh).

These two signals are generated by decoding address lines A19-A12. Note that glitches may be observed on the /RAMCS and /ROMCS signals because the address decoding logic decodes only A19-A12, without any control signals.

Bit D5 of the System Configuration Register allows the option of disabling the /ROMCS signal. This feature is used in systems which, for example, have a shadow RAM. However, prior to disabling the /ROMCS signal, the ROMBR and RAMLBR registers must be re-initialized from their default values.

For more details, please refer to “Programming section”.

ROM Emulator Mode

To ease development, the SAC has a mode to support “ROM emulator” development systems. In this mode, a read data from on-chip registers (except Z181 MPU on-chip registers) are available (data bus direction set to output) to make data visible from the outside, so that a ROM Emulator/Logic Analyzer can monitor internal transactions. Otherwise, a read from an internal transaction is not available to the outside (data bus direction set to Hi-Z status). Mode selection is made through the D1 bit in the System Configuration Register (I/O Address: EDh).

Programming

The following subsections explain and define the parameters for I/O Address assignments, I/O Control Register Addresses and all pertinent Timing parameters.

I/O Address Assignment

The SAC has 78 internal 8-bit registers to control on-chip peripherals and features. Sixty-four registers out of 78 registers are occupied by the Z181 MPU control registers; two for SCC control registers, four for PIA control registers, four for the Counter/Timer, three for RAM/ROM configuration (memory address boundaries) and one for SAC’s system control. The SAC’s I/O addresses are listed in Table 1. These registers are assigned in the SAC’s I/O addressing space and the I/O addresses are fully decoded from A7-A0 and have no image.

PROGRAMMING (Continued)

Table 1. I/O Control Register Address

Address	Register
00h to 3Fh	Z181 MPU Control Registers (Relocatable to 040h-07Fh, or 080h-0BFh)
E0h	PIA1 Data Direction Register (P1DDR)
E1h	PIA1 Data Port (P1DP)
E2h	PIA2 Data Direction Register (P2DDR)
E3h	PIA2 Data Register (P2DP)
E4h	CTC Channel 0 Control Register (CTC0)
E5h	CTC Channel 1 Control Register (CTC1)
E6h	CTC Channel 2 Control Register (CTC2)
E7h	CTC Channel 3 Control Register (CTC3)
E8h	SCC Control Register (SCCCR)
E9h	SCC Data Register (SCCDR)
EAh	RAM Upper Boundary Address Register (RAMUBR)
EBh	RAM Lower Boundary Address Register (RAMLBR)
ECh	ROM Address Boundary Register (ROMBR)
EDh	System Configuration Register (SCR)
EEh	Reserved
EFh	Reserved

Z181 MPU Control Registers

The I/O address for these registers can be relocated in 64 byte boundaries by programming of the I/O Control Register (Address xx111111b).

Do not relocate these registers to address from 0C0h since this will cause an overlap of the Z180 registers and the 16 registers of the Z181 (address 0E0h to 0EFh).

Also, the OMCR register (Address: xx111101b) must be programmed as 0x0xxxxxb (x: don't care) as a part of the initialization procedure. The M1E bit (Bit D7) of this register must be programmed as 0 or the interrupt daisy chain is corrupted. The /IOC bit (Bit D5) of this register is programmed as 0 so that the timing of the /RD and /IORQ signals are compatible with Z80 peripherals.

For detailed information, refer to the Z180 Technical Manual.

ASCI CHANNELS CONTROL REGISTERS

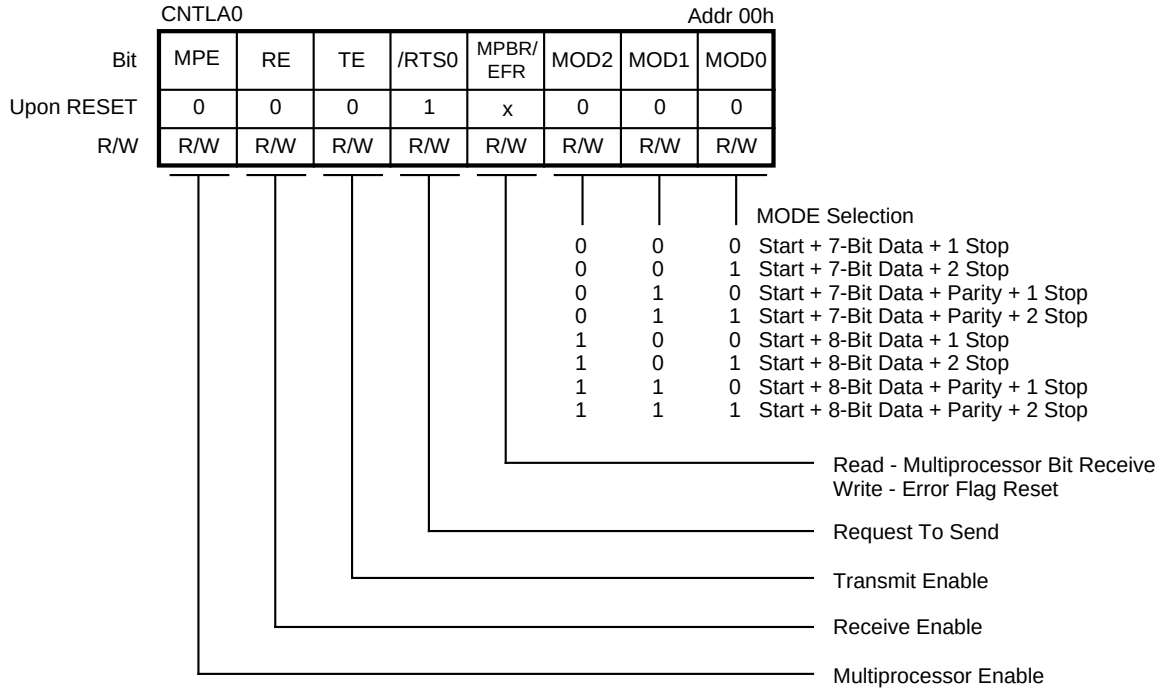


Figure 7. ASCI Control Register A (Ch. 0)

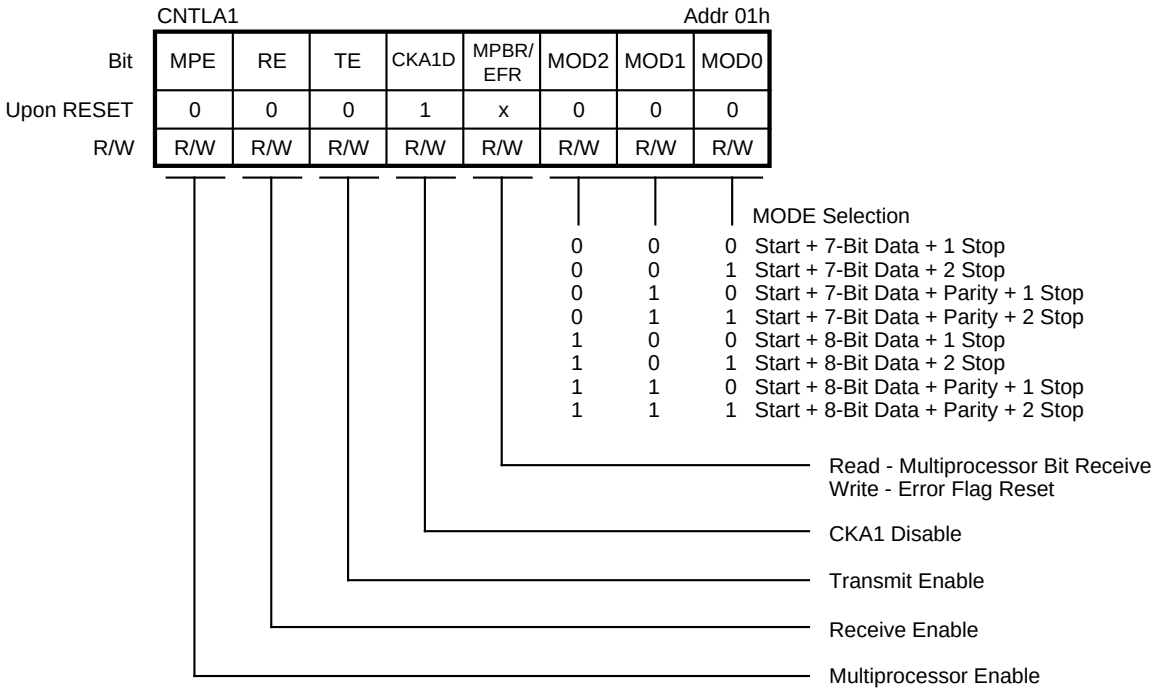
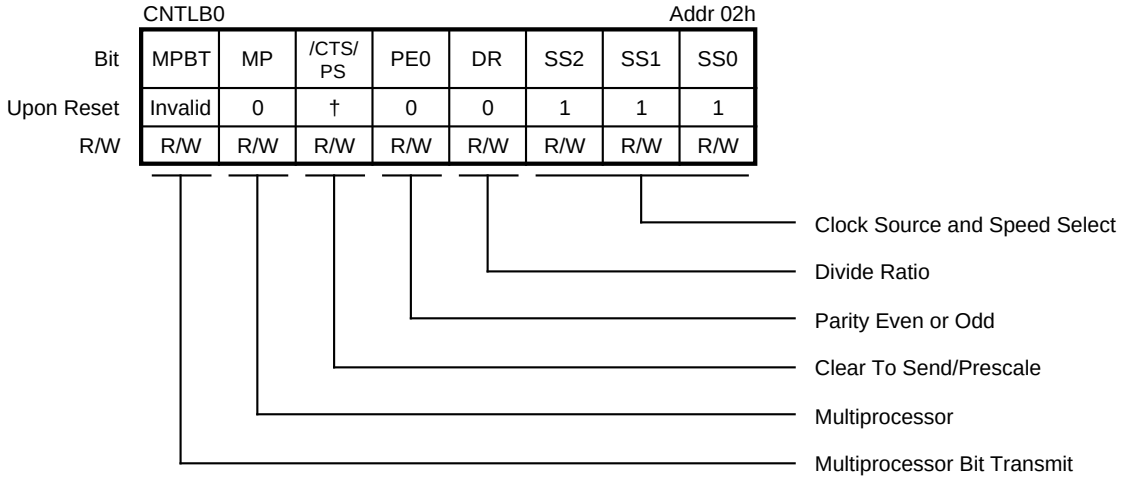


Figure 8. ASCI Control Register A (Ch. 1)

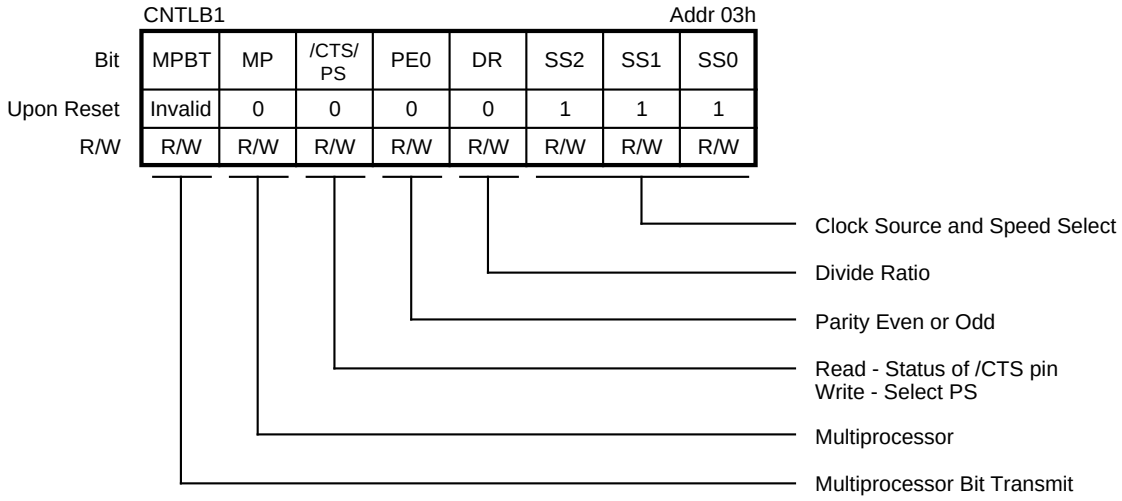


† /CTS - Depending on the condition of /CTS pin.
PS - Cleared to 0.

General Divide Ratio SS, 2, 1, 0	PS = 0 (Divide Ratio = 10) DR = 0 (x16)	DR = 1 (x64)	PS = 1 (Divide Ratio = 30) DR = 0 (x16)	DR = 1 (x64)
000	Ø ÷ 160	Ø ÷ 640	Ø ÷ 480	Ø ÷ 1920
001	Ø ÷ 320	Ø ÷ 1280	Ø ÷ 960	Ø ÷ 3840
010	Ø ÷ 640	Ø ÷ 2580	Ø ÷ 1920	Ø ÷ 7680
011	Ø ÷ 1280	Ø ÷ 5120	Ø ÷ 3840	Ø ÷ 15360
100	Ø ÷ 2560	Ø ÷ 10240	Ø ÷ 7680	Ø ÷ 30720
101	Ø ÷ 5120	Ø ÷ 20480	Ø ÷ 15360	Ø ÷ 61440
110	Ø ÷ 10240	Ø ÷ 40960	Ø ÷ 30720	Ø ÷ 122880
111	External Clock (Frequency < Ø ÷ 40)			

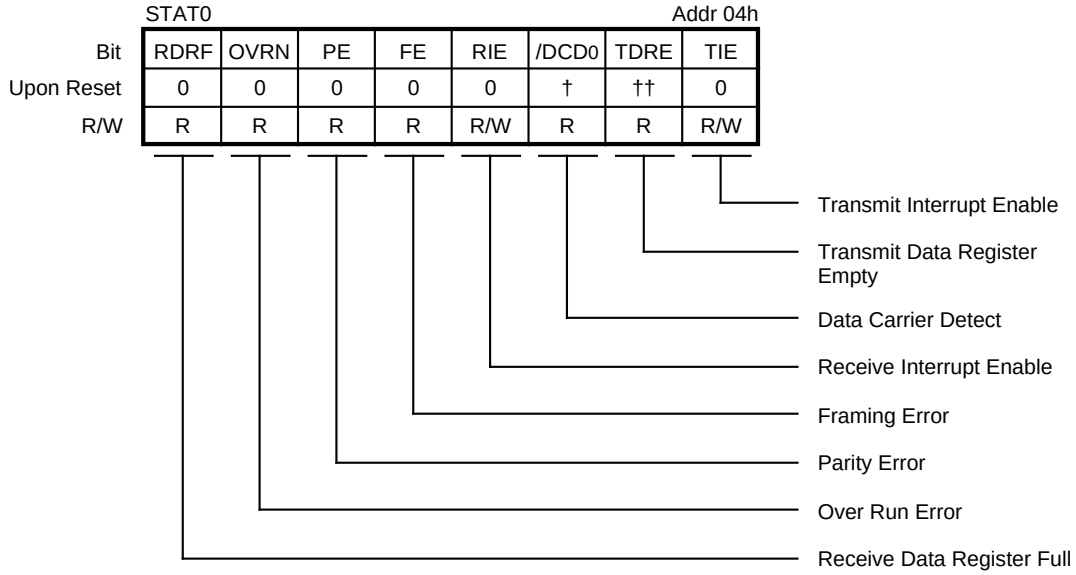
Figure 9. ASCI Control Register B (Ch. 0)

ASCI CHANNELS CONTROL REGISTERS (Continued)



General Divide Ratio SS, 2, 1, 0	PS = 0 (Divide Ratio = 10) DR = 0 (x16)	DR = 1 (x64)	PS = 1 (Divide Ratio = 30) DR = 0 (x16)	DR = 1 (x64)
000	Ø ÷ 160	Ø ÷ 640	Ø ÷ 480	Ø ÷ 1920
001	Ø ÷ 320	Ø ÷ 1280	Ø ÷ 960	Ø ÷ 3840
010	Ø ÷ 640	Ø ÷ 2580	Ø ÷ 1920	Ø ÷ 7680
011	Ø ÷ 1280	Ø ÷ 5120	Ø ÷ 3840	Ø ÷ 15360
100	Ø ÷ 2560	Ø ÷ 10240	Ø ÷ 7680	Ø ÷ 30720
101	Ø ÷ 5120	Ø ÷ 20480	Ø ÷ 15360	Ø ÷ 61440
110	Ø ÷ 10240	Ø ÷ 40960	Ø ÷ 30720	Ø ÷ 122880
111	External Clock (Frequency < Ø ÷ 40)			

Figure 10. ASCI Control Register B (Ch. 1)



† /DCD0 - Depending on the condition of /DCD0 Pin.

†† /CTS0 Pin	TDRE
L	1
H	0

Figure 11. ASCI Status Register

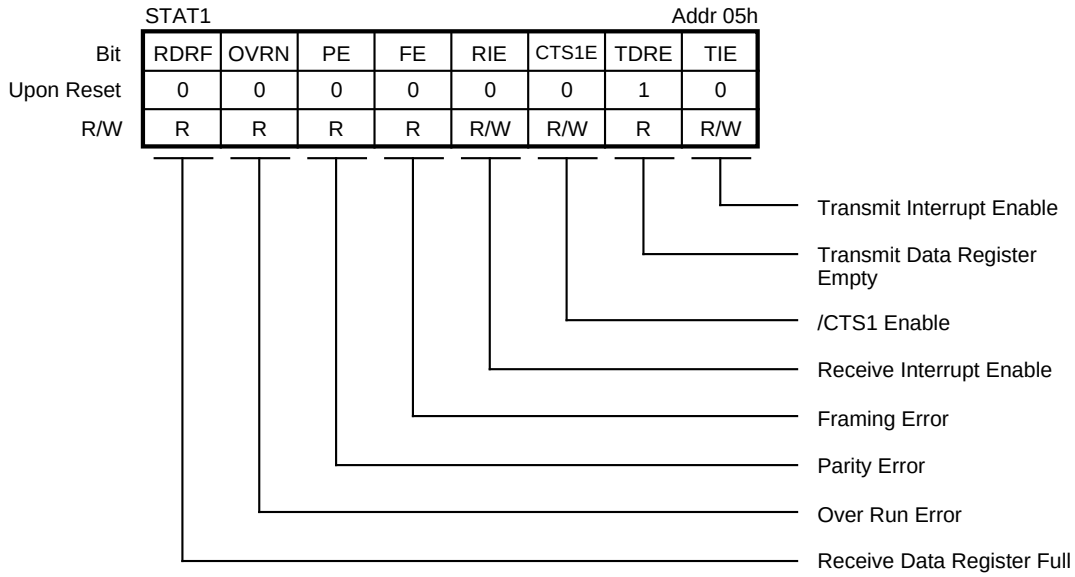


Figure 12. ASCI Status Register (Ch. 1)

ASCI CHANNELS CONTROL REGISTERS (Continued)

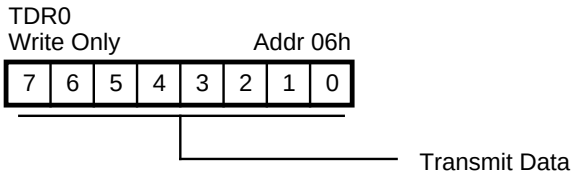


Figure 13. ASCI Transmit Data Register (Ch. 0)

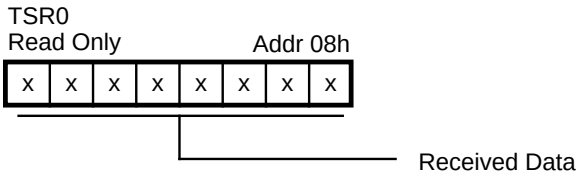


Figure 15. ASCI Receive Data Register (Ch. 0)

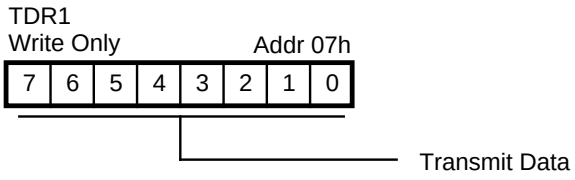


Figure 14. ASCI Transmit Data Register (Ch. 1)

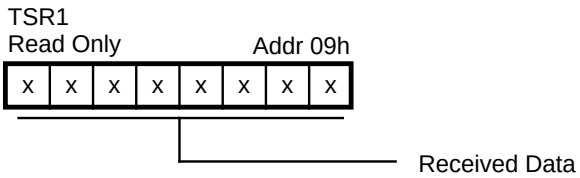
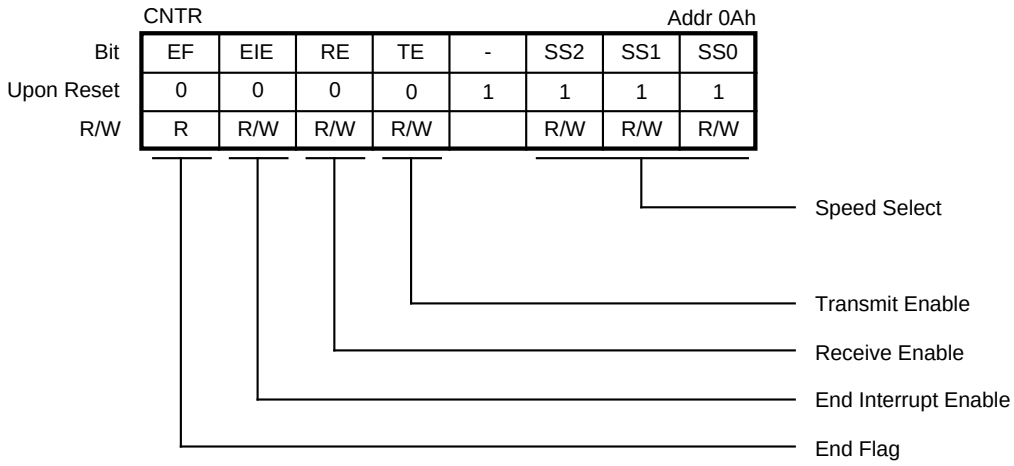


Figure 16. ASCI Receive Data Register (Ch. 1)

CSI/O Registers



SS2, 1, 0	Baud Rate
000	Ø ÷ 20
001	Ø ÷ 40
010	Ø ÷ 80
011	Ø ÷ 100

SS2, 1, 0	Baud Rate
100	Ø ÷ 320
101	Ø ÷ 640
110	Ø ÷ 1280
111	External Clock (Frequency < Ø ÷ 20)

Figure 17. CSI/O Control Register

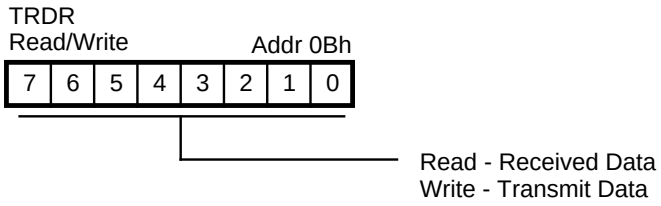


Figure 18. CSI/O Transmit/Receive Data Register

TIMER REGISTERS

Timer Data Registers

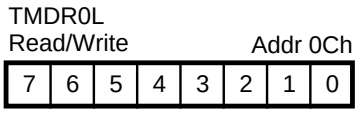
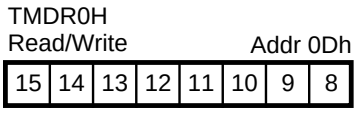


Figure 19. Timer 0 Data Register L



When Read, read Data Register L before reading Data Register H.

Figure 21. Timer 0 Data Register H

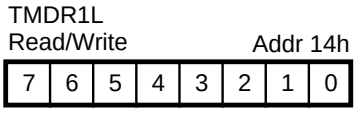
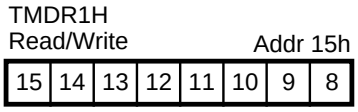


Figure 20. Timer 1 Data Register L



When Read, read Data Register L before reading Data Register H.

Figure 22. Timer 1 Data Register H

Timer Reload Registers

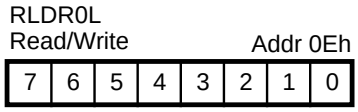


Figure 23. Timer 0 Reload Register L

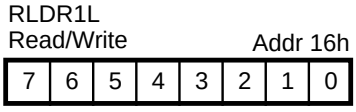


Figure 24. Timer 1 Reload Register L

Timer Reload Registers (Continued)

RLDR0H
Read/Write — Addr 0Fh

15	14	13	12	11	10	9	8

Figure 25. Timer 0 Reload Register H

RLDR1H
Read/Write — Addr 17h

15	14	13	12	11	10	9	8

Figure 26. Timer 1 Reload Register H

Timer Control Register

TCR — Addr 10h

Bit	TIF1	TIF0	TIE1	TIE0	TOC1	TOC0	TDE1	TDE0
Upon Reset	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Timer Down Count Enable 1,0
Timer Output Control 1,0
Timer Interrupt Enable 1,0
Timer Interrupt Flag 1,0

TOC1,0	A15/TOUT
00	Inhibited
01	Toggle
10	0
11	1

Figure 27. Timer Control Register

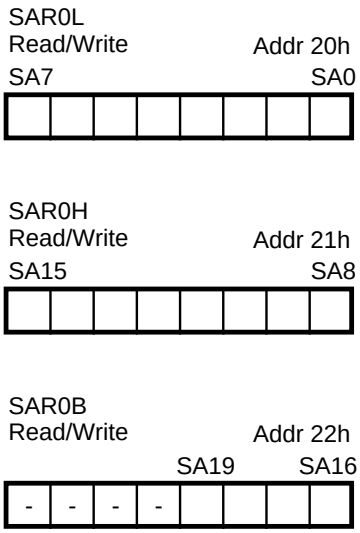
Free Running Counter

FRC
Read Only — Addr 18h

7	6	5	4	3	2	1	0

Figure 28. Free Running Counter

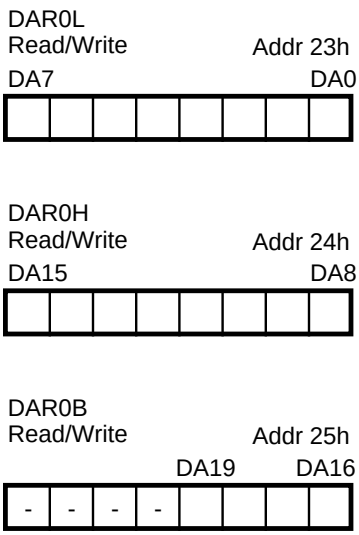
DMA Registers



Bits 0-2 (3) are used for SAR0B

A19,	A18,	A17,	A16	DMA Transfer Request
x	x	0	0	/DREQ0 (external)
x	x	0	1	RDR0 (ASCI0)
x	x	1	0	TDR0 (ASCI1)
x	x	1	1	Not Used

Figure 29. DMA 0 Source Address Registers



Bits 0-2 (3) are used for DAR0B

A19,	A18,	A17,	A16	DMA Transfer Request
x	x	0	0	/DREQ0 (external)
x	x	0	1	RDR0 (ASCI0)
x	x	1	0	TDR0 (ASCI1)
x	x	1	1	Not Used

Figure 30. DMA 0 Destination Address Registers

DMA REGISTERS (Continued)

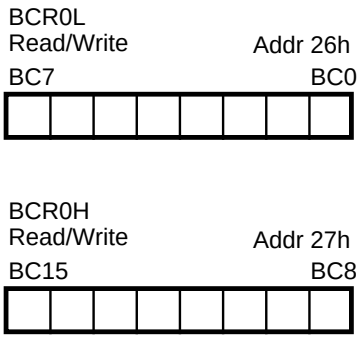


Figure 31. DMA 0 Byte Counter Registers

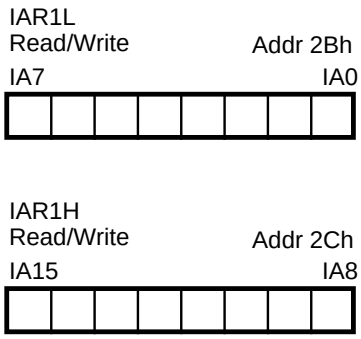


Figure 33. DMA 1 I/O Address Registers

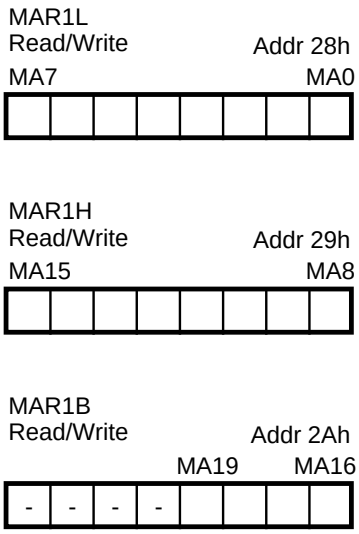


Figure 32. DMA 1 Memory Address Registers

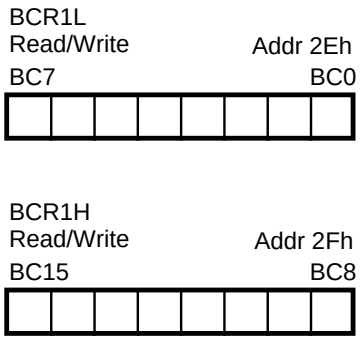


Figure 34. DMA 1 Byte Count Registers

DSTAT — Addr 30h

Bit	DE1	DE0	/DWE1	/DWE0	DIE1	DIE0	-	DIME
Upon Reset	0	0	1	1	0	0	1	0
R/W	R/W	R/W	W	W	R/W	R/W		R

DIME — DMA Master Enable
DIE1 — DMA Interrupt Enable 1, 0
/DWE1 — DMA Enable Bit Write Enable 1, 0
DE1 — DMA Enable Ch 1, 0

Figure 35. DMA Status Register

DMODE — Addr 31h

Bit	-	-	DM1	DM0	SM1	SM0	MMOD	-
Upon Reset	1	1	0	0	0	0	0	1
R/W			R/W	R/W	R/W	R/W	R/W	

MMOD — Memory MODE Select
SM1 — Ch 0 Source Mode 1, 0
DM1 — Ch 0 Destination Mode 1, 0

DM1, 0	Destination	Address
00	M	DAR0+1
01	M	DAR0-1
10	M	DAR0 Fixed
11	I/O	DAR0 Fixed

SM1, 0	Source	Address
00	M	SAR0+1
01	M	SAR0-1
10	M	SAR0 Fixed
11	I/O	SAR0 Fixed

MMOD	Mode
0	Cycle Steal Mode
1	Burst Mode

Figure 36. DMA Mode Registers

DMA REGISTERS (Continued)

DCNTL — Addr 32h

Bit	MWI1	MWI0	IWI1	IWI0	DMS1	DMS0	DIM1	DIM0
Upon Reset	1	1	1	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DIM1, 0 — DMA Ch 1 I/O Memory Mode Select

DMS1, 0 — /DREQi Select, i = 1, 0

IWI1, 0 — I/0 Wait Insertion

MWI1, 0 — Memory Wait Insertion

MWI1, 0	No. of Wait States
00	0
01	1
10	2
11	3

IWI1, 0	No. of Wait States
00	0
01	2
10	3
11	4

DMSi	Sense
1	Edge Sense
0	Level Sense

DM1, 0	Transfer Mode	Address Increment/Decrement	
00	M - I/O	MAR1+1	IAR1 Fixed
01	M - I/O	MAR1-1	IAR1 Fixed
10	I/O - M	IAR1 Fixed	MAR1+1
11	I/O - M	IAR1 Fixed	MAR1-1

Figure 37. DMA/WAIT Control Register

MMU Registers

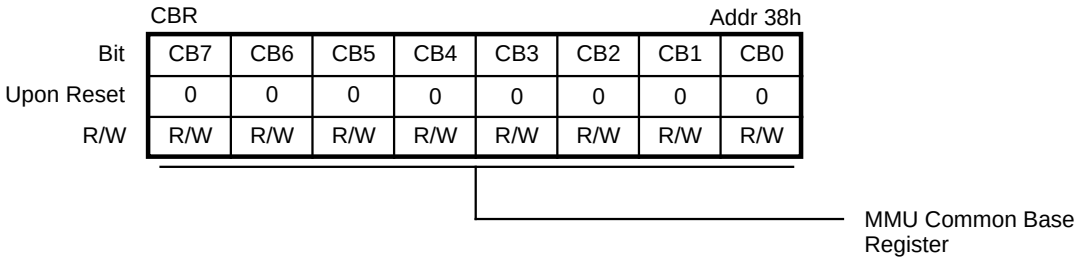


Figure 38. MMU Common Base Register

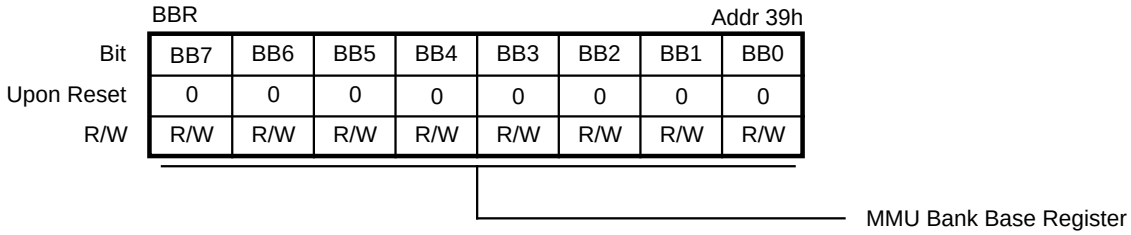


Figure 39. MMU Bank Base Register

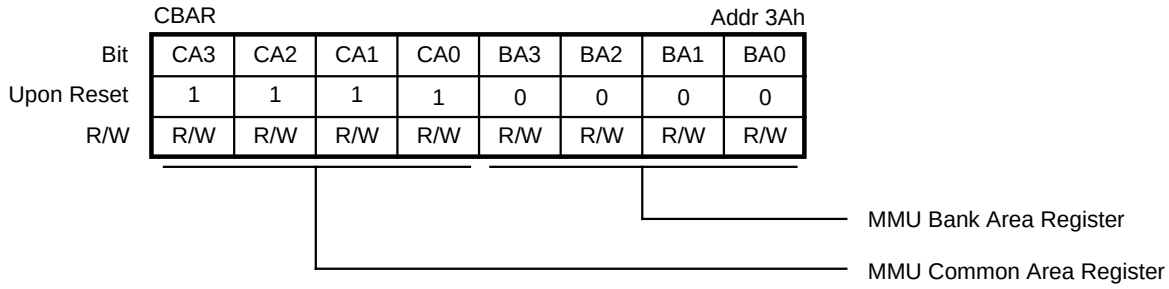


Figure 40. MMU Common/Bank Area Register

System Control Registers

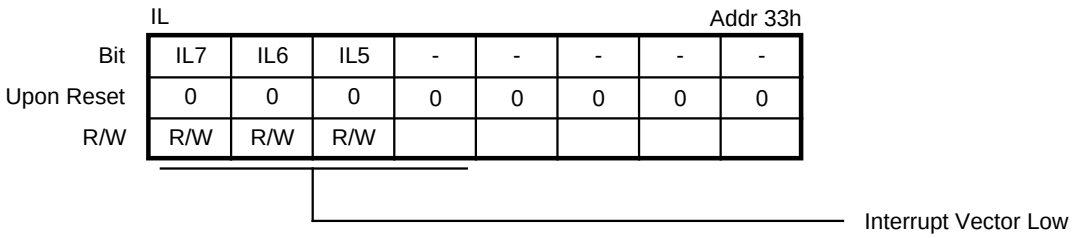


Figure 41. Interrupt Vector Low Register

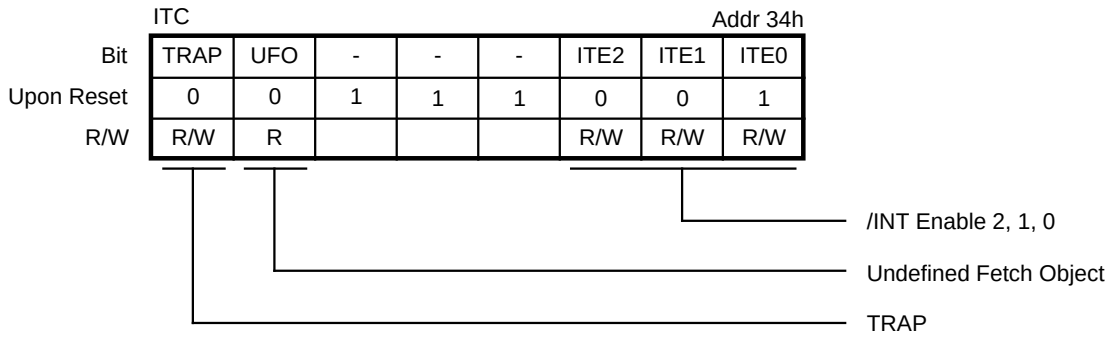
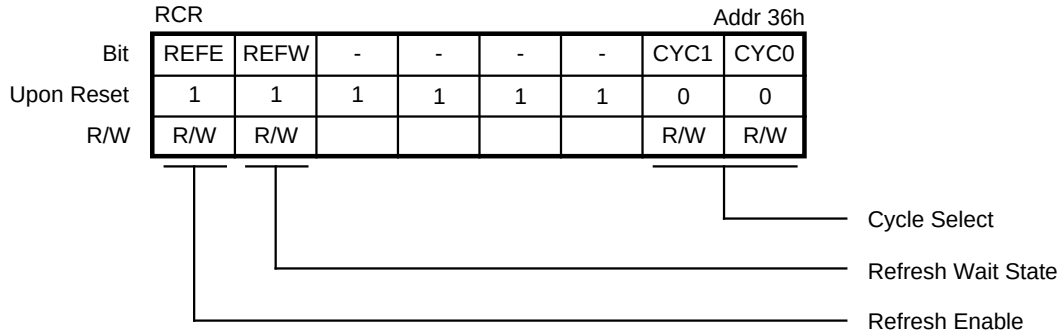
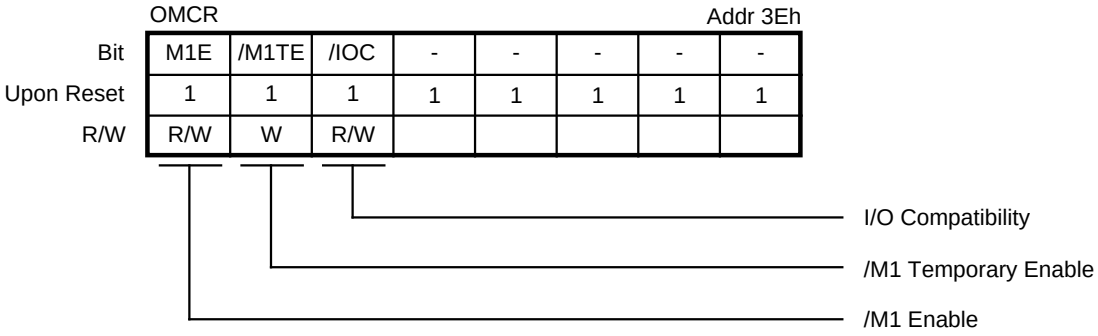


Figure 42. INT/TRAP Control Register



CYC1, 0	Interval of Refresh Cycle
00	10 states
01	20 states
10	40 states
11	80 states

Figure 43. Refresh Control Register



Note: This register has to be programmed as 0x0xxxxxb(x:don't care) as a part of Initialization.

Figure 44. Operation Mode Control Register

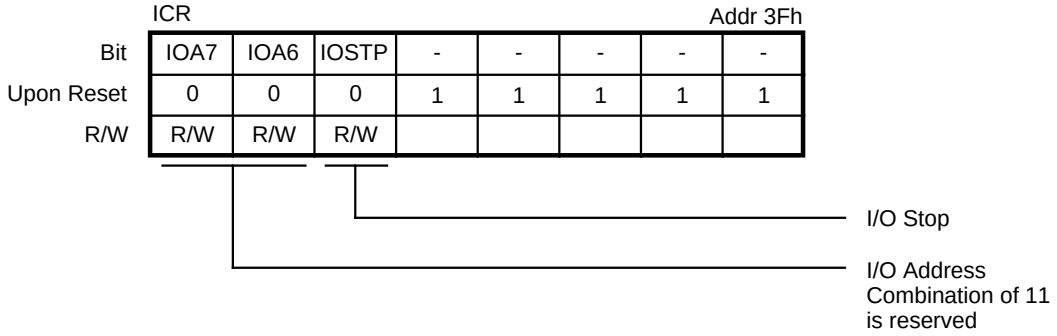


Figure 45. I/O Control Register

CTC Control Registers

Channel Control Word

This word sets the operating modes and parameters as described below. Bit D0 must be a "1" to indicate that this is a Control Word (Figure 46).

For more detailed information, refer to the CTC Technical Manual.

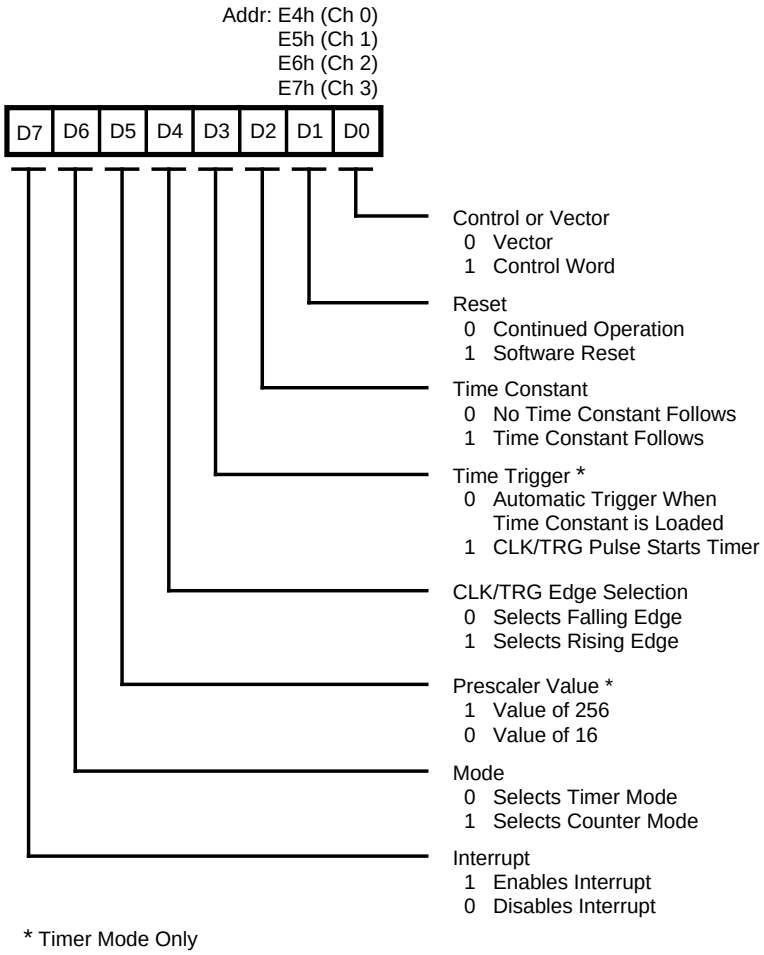


Figure 46. CTC Channel Control Word

This register has the following fields:

Bit D7. *Interrupt Enable.* This bit enables the interrupt logic so that an internal INT is generated at zero count. Interrupts are programmed in either mode and may be enabled or disabled at any time.

Bit D6. *Mode Bit.* This bit selects either Timer Mode or Counter Mode.

Bit D5. *Prescaler Factor.* This bit selects the prescaler factor for use in the timer mode. Either divide-by-16 or divide-by-256 is available.

Bit D4. *Clock/Trigger Edge Selector.* This bit selects the active edge of the CLK/TRG input pulses.

Bit D3. *Timer Trigger.* This bit selects the trigger mode for timer operation. Either automatic or external trigger may be selected.

Bit D2. *Time Constant.* This bit indicates that the next word programmed is time constant data for the downcounter.

Bit D1. *Software Reset.* Writing a "1" to this bit indicates a software reset operation, which stops counting activities until another time constant word is written.

Time Constant Word

Before a channel can start counting, it must receive a time constant word. The time constant value may be anywhere between 1 and 256, with "0" being accepted as a count of 256 (Figure 47).

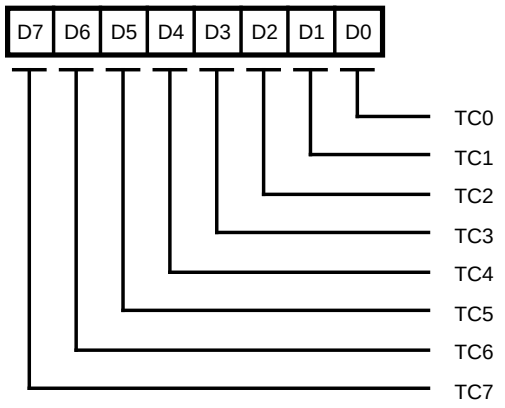


Figure 47. CTC Time Constant Word

Interrupt Vector Word

If one or more of the CTC channels have interrupt enabled, then the Interrupt Vector Word is programmed. Only the five most significant bits of this word are programmed, and bit D0 must be "0". Bits D2-D1 are automatically modified by the CTC channels after responding with an interrupt vector (Figure 48).

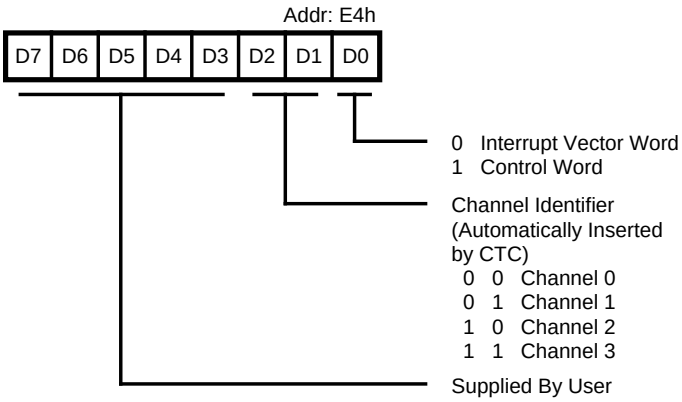


Figure 48. CTC Interrupt Vector Word

SCC REGISTERS

For more detailed information, please refer to the Z8030/ Z8530 SCC Technical Manual.

Note:
The Address for the Control/Status Register is E8h. The Address for the Data Register is E9h.

Read Registers

The SCC contains eight read registers. To read the contents of a register (rather than RR0), the program must first initialize a pointer to WR0 in exactly the same manner as a write operation. The next I/O read cycle will place the contents of the selected read registers onto the data bus (Figure 49).

Table 2. SCC Read Registers

Bit	Description
RR0	Transmit and Receive buffer status and external status.
RR1	Special Receive Condition status.
RR2	Interrupt vector (modified if VIS Bit in WR9 is set).
RR3	Interrupt pending bits.
RR6	SDLC FIFO byte counter lower byte (only when enabled).
RR7	SDLC FIFO byte count and status (only when enabled).
RR8	Receive buffer.
RR10	Miscellaneous status bits.
RR12	Lower byte of baud rate.
RR13	Upper byte of baud rate generator time constant.
RR15	External Status interrupt information.

SCC REGISTERS (Continued)

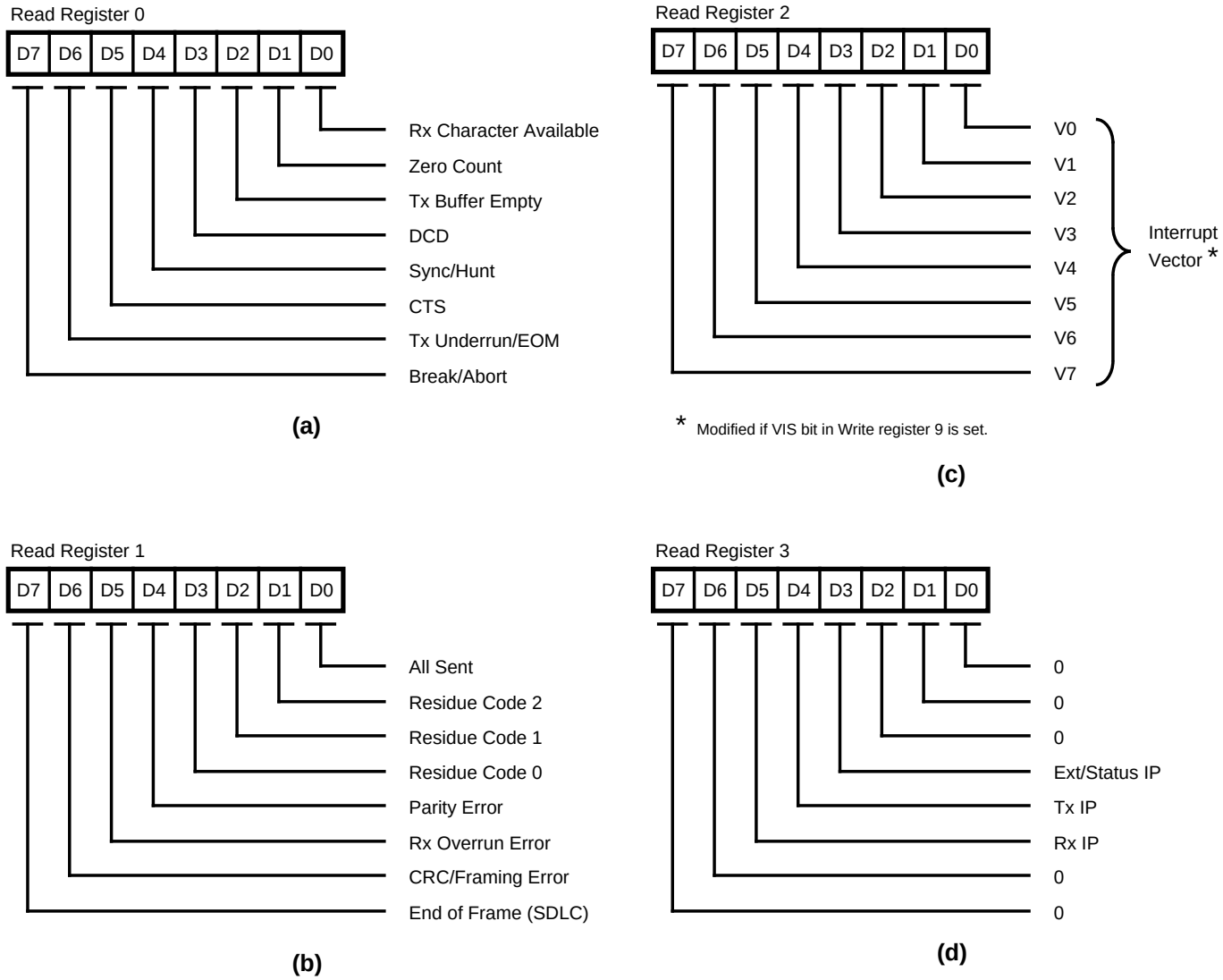
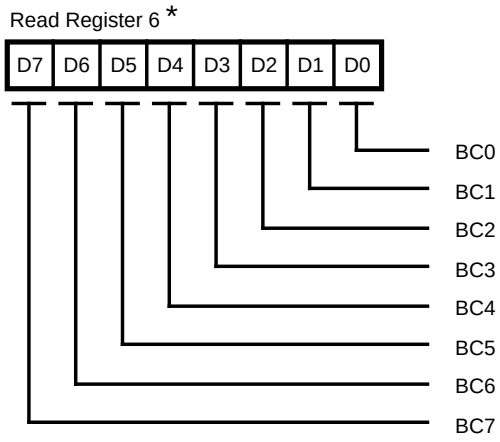
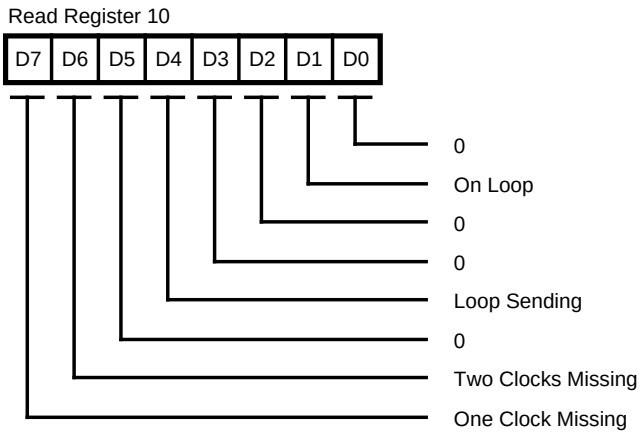


Figure 49. SCC Read Register Bit Functions

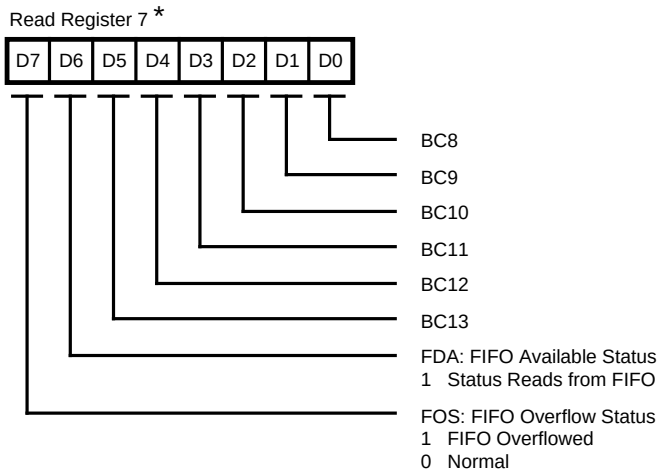


* Can only be accessed if the SDLC FIFO enhancement is enabled (WR15 bit D2 set to 1)

(e) SDLC FIFO Status and Byte Count (LSB)

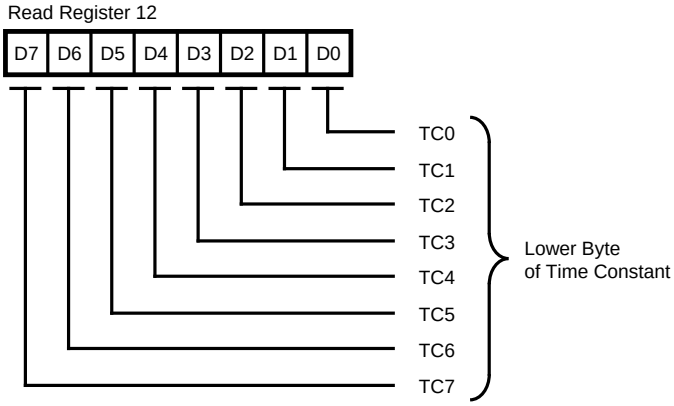


(g)



* Can only be accessed if the SDLC FIFO enhancement is enabled (WR15 bit D2 set to 1)

(f) SDLC FIFO Status and Byte Count (MSB)



(h)

Figure 49. SCC Read Register Bit Functions (Continued)

SCC REGISTERS (Continued)

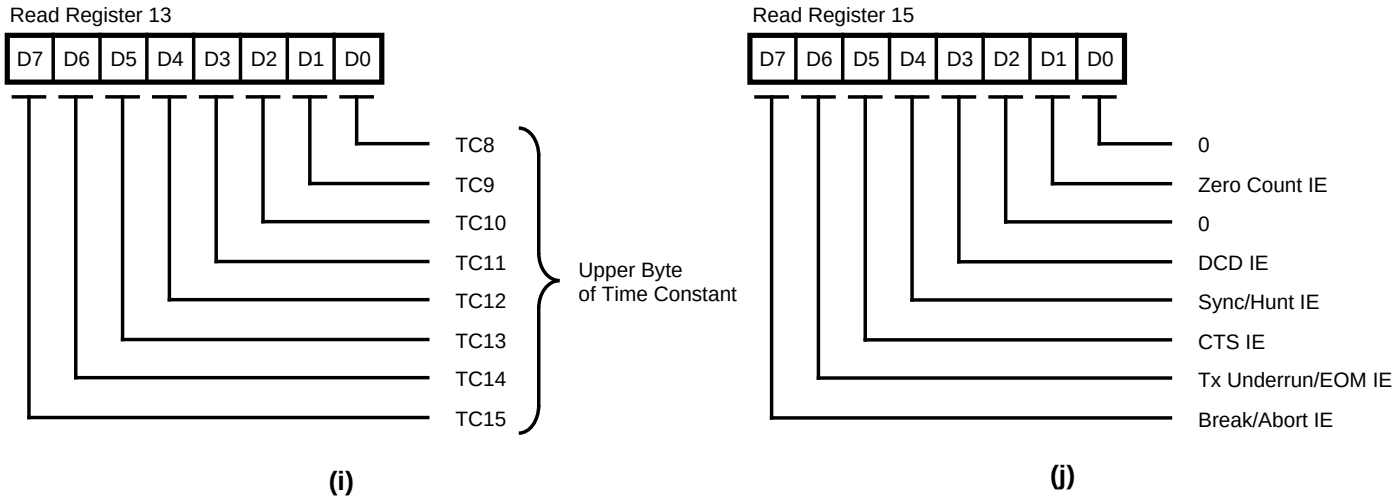


Figure 49. SCC Read Register Bit Functions (Continued)

Write Registers

The SCC contains fifteen write registers that are programmed to configure the operating modes of the channel. With the exception of WR0, programming the write registers is a two step operation. The first operation is a pointer written to WR0 that points to the selected register. The second operation is the actual control word that is written into the register to configure the SCC channel (Figure 50).

Table 3. SCC Write Registers

Bit	Description
WR0	Register Pointers, various initialization commands
WR1	Transmit and Receive interrupt enables, WAIT/DMA commands
WR2	Interrupt Vector
WR3	Receive parameters and control modes
WR4	Transmit and Receive modes and parameters
WR5	Transmit parameters and control modes
WR6	Sync Character or SDLC address
WR7	Sync Character or SDLC flag

Bit	Description
WR8	Transmit buffer
WR9	Master Interrupt control and reset commands
WR10	Miscellaneous transmit and receive control bits
WR11	Clock mode controls for receive and transmit
WR12	Lower byte of baud rate generator
WR13	Upper byte of baud rate generator
WR14	Miscellaneous control bits
WR15	External status interrupt enable control

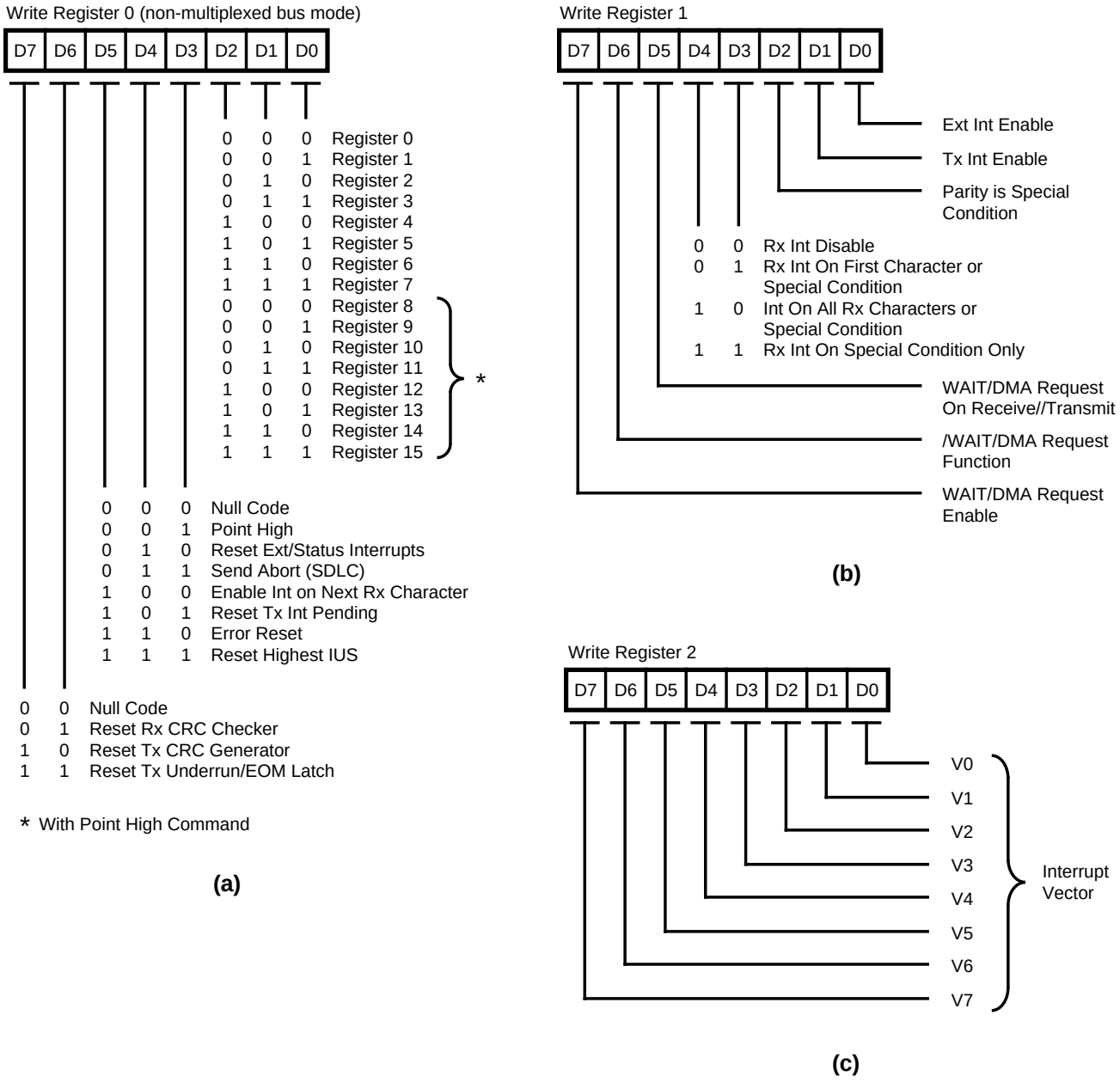


Figure 50. Write Register Bit Functions

SCC REGISTERS (Continued)

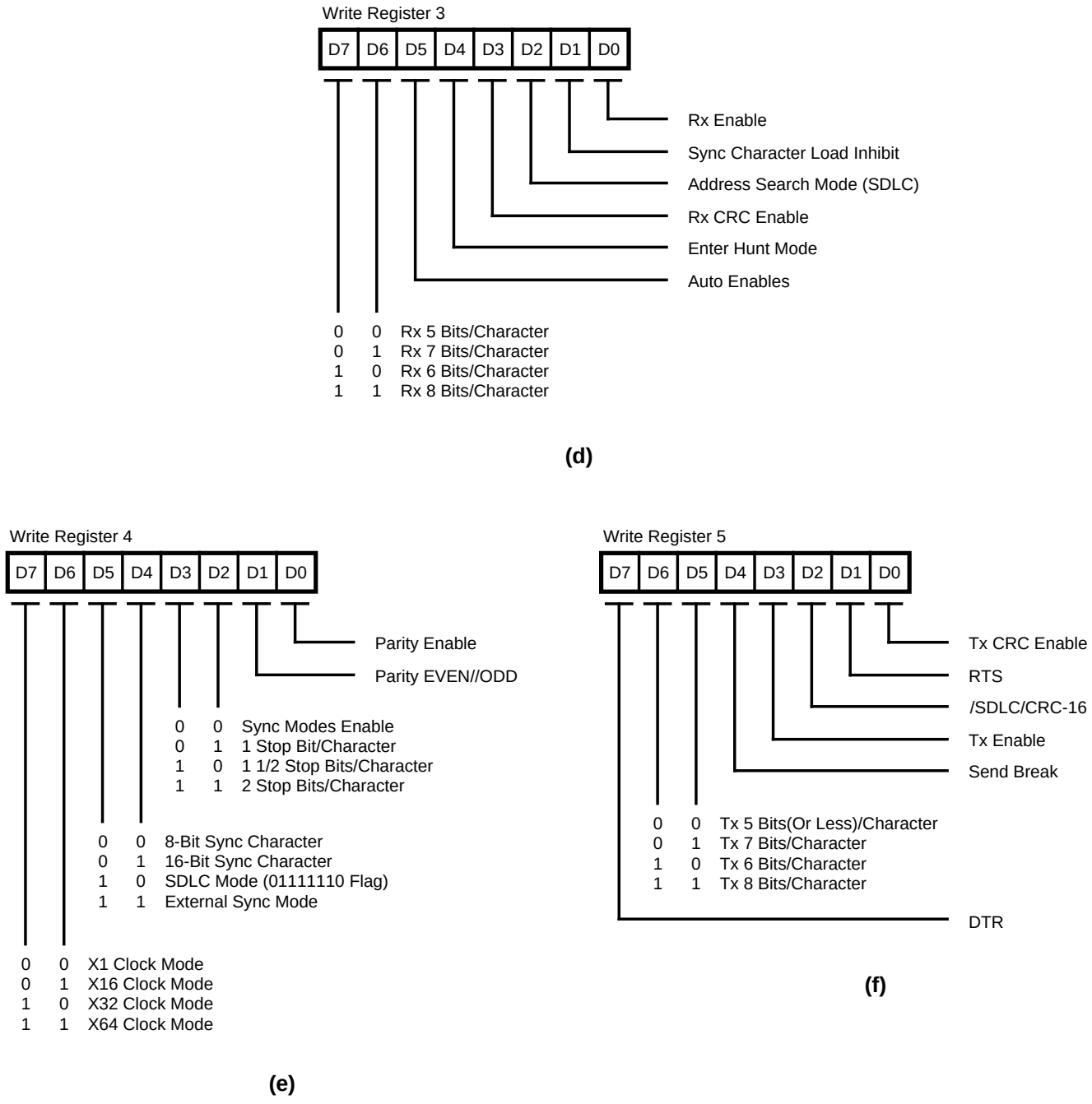
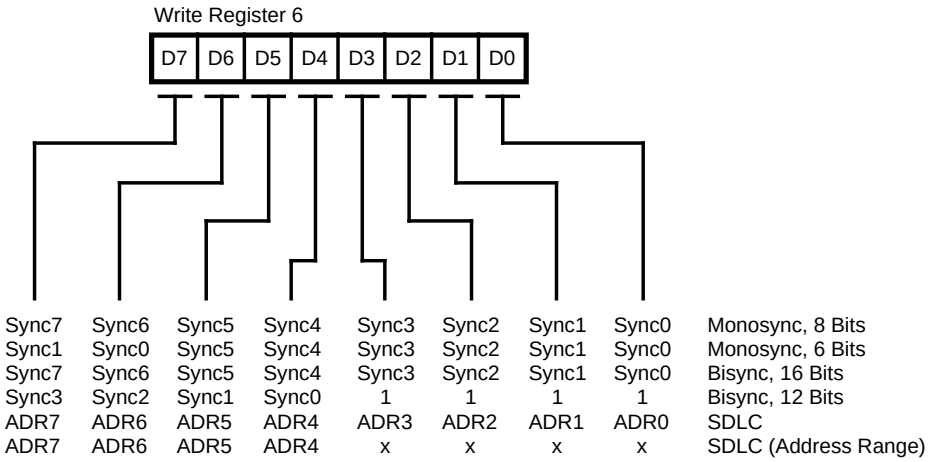
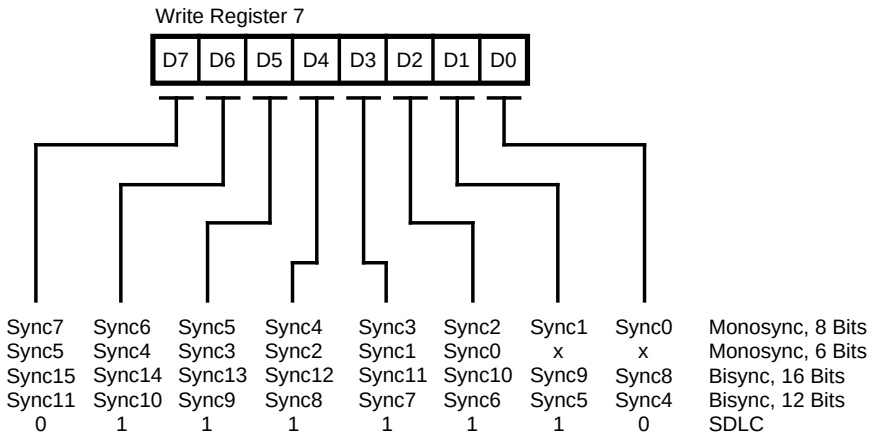


Figure 50. Write Register Bit Functions (Continued)



(g)



(h)

Figure 50. Write Register Bit Functions (Continued)

SCC REGISTERS (Continued)

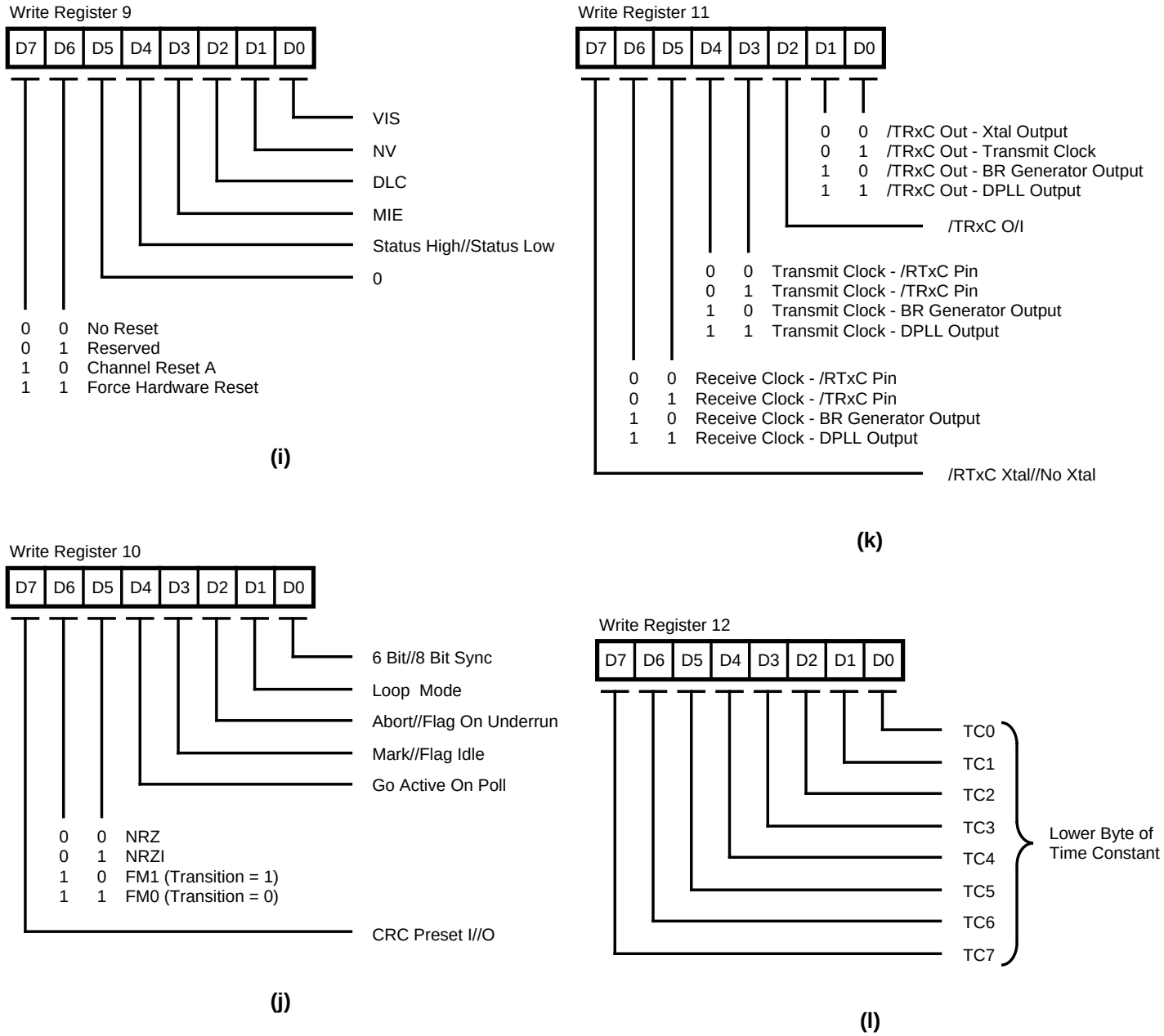
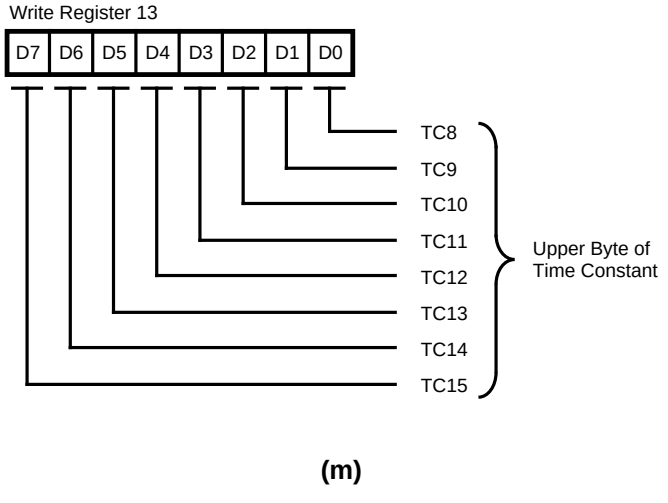
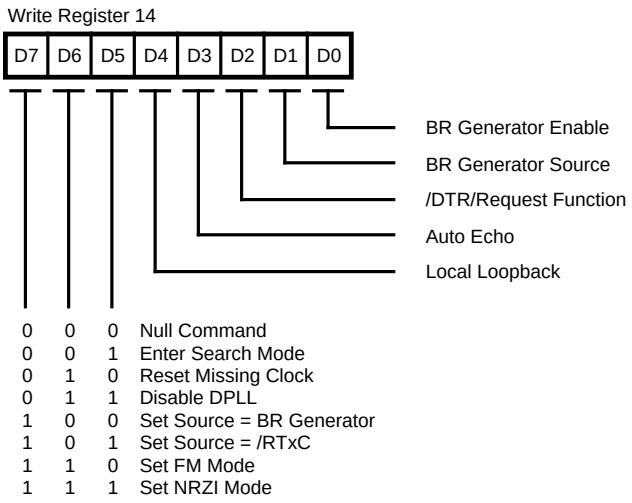


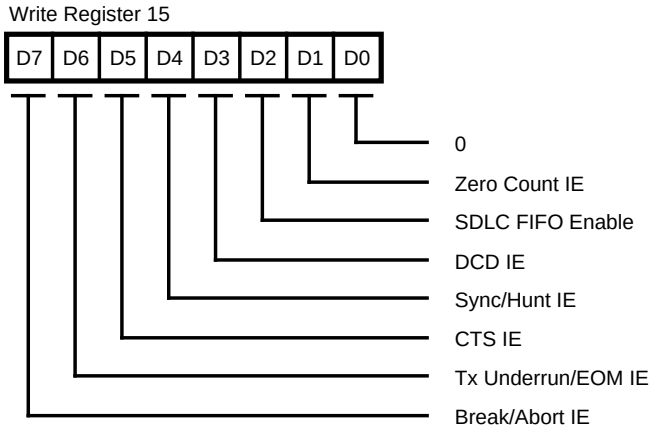
Figure 50. Write Register Bit Functions (Continued)



(m)



(n)



(o)

Figure 50. Write Register Bit Functions (Continued)

PIA Control Registers

PIA1 Data Direction Register (P1DDR, I/O Address E0h), PIA1 Data Port (P1DP, I/O address E1h), PIA2 Data Direction Register (P2DDR, I/O Address E2h) and PIA2 Data Register (P2DP, I/O Address E3h). These four registers are shown in Figures 51-54. Note that if the CTC/PIA bit in the System Configuration Register is set to one, the CTC I/O functions override the PIA1 function, and programming of P1DDR is ignored.

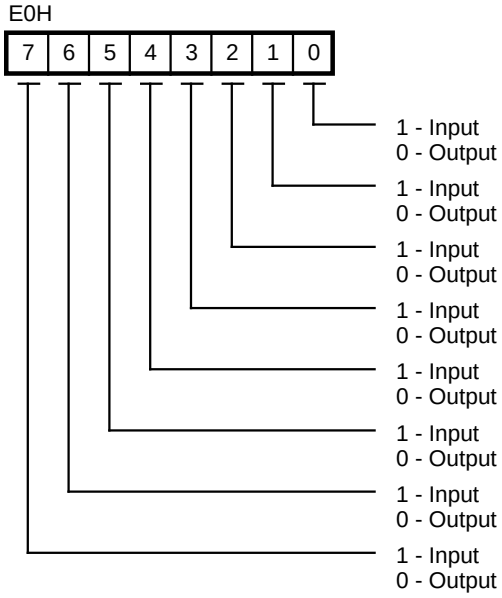


Figure 51. PIA 1 Data Direction Register

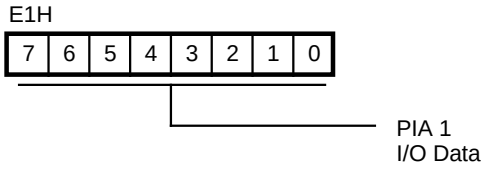


Figure 52. PIA 1 Data Register

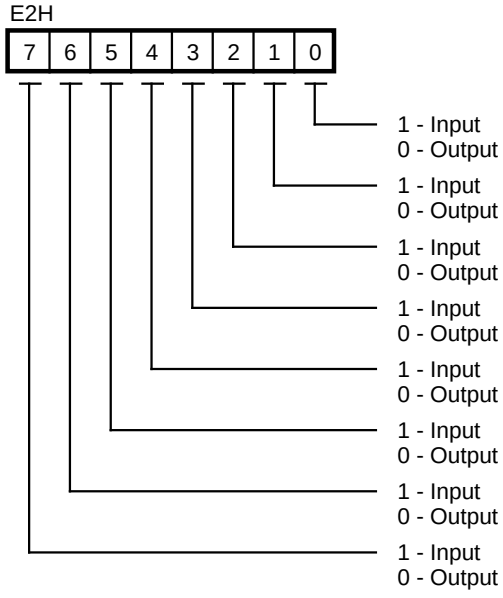


Figure 53. PIA 2 Data Direction Register

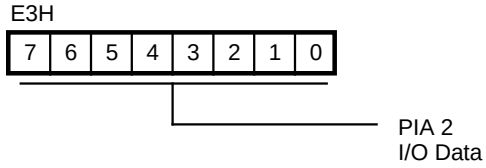


Figure 54. PIA 2 Data Register

The Data Port is the register to/from the 8-bit parallel port. At power on Reset, they are initialized to 1.

The Data Direction Register has eight control bits. Individual bits specify each bit's direction. When the bit is set to a "1", the bit becomes an input, otherwise it is an output. On reset, these registers are initialized to 1, resulting in all lines being inputs.

REGISTERS FOR SYSTEM CONFIGURATION

There are four registers to determine system configuration with the Z181. These registers are: RAM upper boundary address register (RAMUBR, I/O address EAh), RAM lower boundary address register (RAMLBR, I/O address EBh), ROM address boundary register (ROMBR, I/O address ECh) and System Configuration Register (SCR, I/O address EDh).

ROM Address Boundary Register (ROMBR, I/O Address ECh)

This register specifies the address range for the /ROMCS signal. When accessed memory addresses are less than or equal to the value programmed in this register, the /ROMCS signal is asserted (Figure 55).

The A18 signal from the CPU is obtained before it is multiplexed with "TOUT". This signal can be forced to "1" (inactive state) by setting Bit D5 of the System Configuration Register, to allow the user to overlay the RAM area over the ROM area. At power-up reset, this register contains all 1's so that /ROMCS is asserted for all addresses.

RAM Lower Boundary Address Register (RAMLBR, I/O Address EBh) and RAM Upper Boundary Address Register (RAMUBR, I/O Address EAh)

These two registers specify the address range for the /RAMCS signal. When accessed memory addresses are less than or equal to the value programmed in the RAMUBR and greater than or equal to the value programmed in the RAMLBR, /RAMCS is asserted. (Figure 13) The A18 signal from the CPU is taken before it is multiplexed with "T_{OUT}". In the case that these register are programmed to overlap, /ROMCS takes priority over /RAMCS (/ROMCS is asserted and /RAMCS is inactive).

Chip Select signals are going active for the address range:

/ROMCS: (ROMBR) ≥ A19-A12 ≥ 0
/RAMCS: (RAMUBR) ≥ A19-A12 > (RAMLBR)

These registers are set to "FFh" at power-on Reset, and the boundary addresses of ROM and RAM are the following:

ROM lower boundary address
(fixed) = 00000h

ROM upper boundary address
(ROMBR register) = 0FFFFFh

RAM lower boundary address
(RAMLBR register) = 0FFFFFh

RAM upper boundary address
(RAMUBR register) = 0FFFFFh

Since /ROMCS takes priority over /RAMCS, the latter will never be asserted until the value in the ROMBR and RAMLBR registers are re-initialized to lower values.

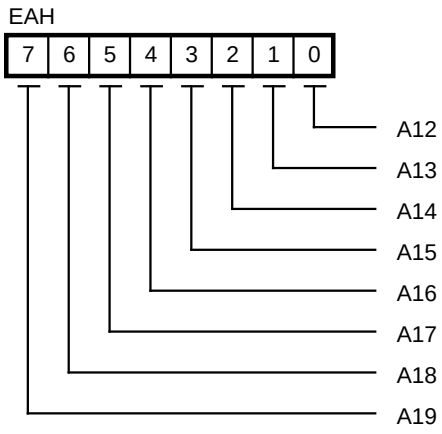


Figure 55. RAM Upper Boundary Register

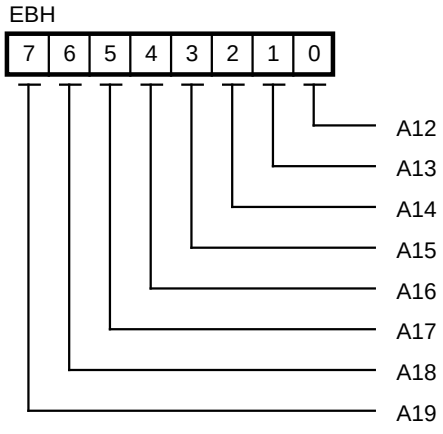


Figure 56. RAM Lower Boundary Register

REGISTERS FOR SYSTEM CONFIGURATION (Continued)

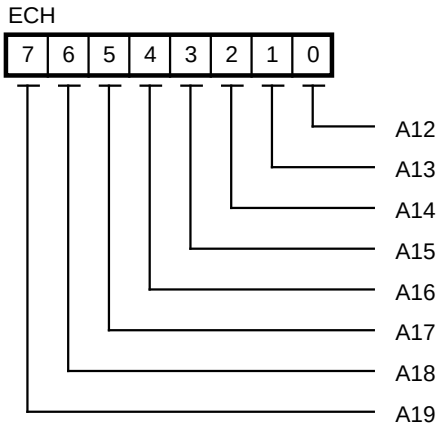


Figure 57. ROM Boundary Register

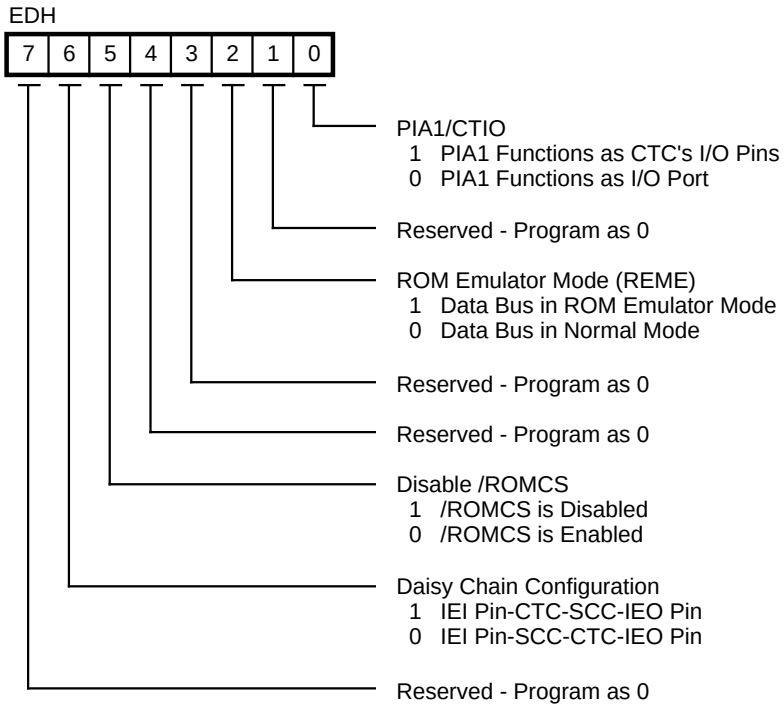


Figure 58. System Configuration Register

System Configuration Register (I/O address EDh)
This register is to determine the functionality of PIA1 and the Interrupt Daisy-Chain Configuration (Figure 13). This register has the following control bits:

Bit D7. Reserved and should be programmed as "0".

Bit D6. *Daisy-Chain Configuration.* Determines the arrangement of the interrupt priority daisy chain.

When this bit is set to "1", priority is as follows:

IEI pin - CTC - SCC - IEO pin

When this bit is "0", priority is as follows:

IEI pin - SCC - CTC - IEO pin

This bit's default (after Reset) is 0.

Bit D5. *Disable /ROMCS.* When this bit is set to "1". /ROMCS is forced to a "1" regardless of the status of the address decode logic. This bit's default (after Reset) is 0 and /ROMCS function is enabled.

Bit D4-D3. Reserved and should be programmed as "00".

Bit D2. *ROM Emulator Mode Enable.* When this bit is set to a 1, the Z181 is in "ROM emulator mode". In this mode, bus direction for certain transaction periods are set to the opposite direction to export internal bus transactions outside the Z80181. This allows the use of ROM emulators/ logic analyzers for applications development. This bit's default (after Reset) is 0.

Bit D1. Reserved and shall be programmed as "0".

Bit D0. *CTC/PIA1.* When this bit is set to "1", PIA1 functions as the CTC's I/O pins. This bit's default (after Reset) is 0.

Data Bus Direction

Table 4 shows the state of the SAC's data bus when in SAC bus master condition.

Table 4. Data Bus Direction (Z181 Is Bus Master)

I/O And Memory Transactions

	I/O Write To On-Chip Peripherals (SCC/CTC/ PIA1/PIA2)	I/O Read From On-Chip Peripherals (SCC/CTC/ PIA1/PIA2)	I/O Write To Off-Chip Peripheral	I/O Read From Off-Chip Peripheral	Write To Memory	Read From Memory	Refresh	Z80181 Idle Mode
Z80181 Data Bus (REME Bit = 0)	Out	Z	Out	In	Out	In	Z	Z
Z80181 Data Bus (REME Bit = 1)	Out	Out	Out	In	Out	In	Z	Z

Interrupt Acknowledge Transaction

	Intack For On-Chip Peripheral (SCC/CTC)	Intack For Off-Chip Peripheral
Z80181 Data Bus (REME Bit = 0)	Z	In
Z80181 Data Bus (REME Bit = 1)	Out	In

Table 5 shows the state of the SAC's data bus when the Z80181 is NOT in bus master condition.

Table 5. Data Bus Direction for External Bus Master (Z80181 Is Not Bus Master)

I/O And Memory Transactions

	I/O Write To On-Chip Peripherals (SCC/CTC/ PIA1/PIA2)	I/O Read From On-Chip Peripherals (SCC/CTC/ PIA1/PIA2)	I/O Write To Off-Chip Peripheral	I/O Read From Off-Chip Peripheral	Write To Memory	Read From Memory	Refresh	Z80181 Idle Mode
Z80181 Data Bus (REME Bit = 0)	In	Out	Z	Z	Z	In	Z	Z
Z80181 Data Bus (REME Bit = 1)	In	Out	Z	Z	Z	In	Z	Z

Interrupt Acknowledge Transaction

	Intack For On-Chip Peripheral (SCC/CTC)	Intack For Off-Chip Peripheral
Z80181 Data Bus (REME Bit = 0)	Out	In
Z80181 Data Bus (REME Bit = 1)	Out	In

The word "OUT" means that the Z181 data bus direction is in output mode, "IN" means input mode, and "HI-Z" means high impedance.

"REME" stands for "ROM Emulator Mode" and is the status of D2 bit in the System Configuration Register.

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} with respect to V_{SS} ..... –0.3V to +7.0V
Voltages on all inputs
with respect to V_{SS} ..... –0.3V to V_{CC} +0.3V
Storage Temperature .....–65°C to +150°C
Operating Ambient
Temperature ..... See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Figure 59).

Available operating
temperature range is: E = –40°C to +100°C

Voltage Supply Range: +4.50V ≤ Vcc ≤ + 5.50V

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pF.

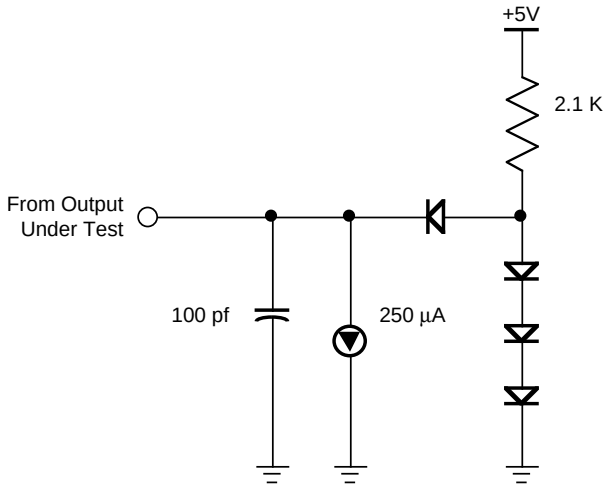


Figure 59. Standard Test Circuit

DC CHARACTERISTICS
Z80181

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH1}	Input "H" Voltage /RESET, EXTAL, /NMI	V_{CC} –0.6		V_{CC} +0.3	V	
V_{IH2}	Input "H" Voltage Except /RESET, EXTAL, /NMI	2.0		V_{CC} +0.3	V	
V_{IL1}	Input "L" Voltage /RESET, EXTAL, /NMI	–0.3		0.6	V	
V_{IL2}	Input "L" Voltage Except /RESET, EXTAL, /NMI	–0.3		0.8	V	
V_{OH}	Output "H" Voltage All outputs.	2.4 V_{CC} –1.2			V	I_{OH} = -200 µA I_{OH} = – 20 µA
V_{OL}	Output "L" Voltage All outputs.			0.45	V	I_{OL} = 2.2 mA
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL			10	µA	V_{IN} = 0.5 – V_{CC} –0.5
I_{TL}	Tri-State Leakage Current			10	µA	V_{IN} = 0.5 – V_{CC} –0.5
I_{CC}*	Power Dissipation* (Normal Operation)		25	80		f = 10 MHz
	Power Dissipation* (SYSTEM STOP mode)		6.3	40		f = 10 MHz
Cp	Pin Capacitance			12	pF	V_{IN} = 0V, f = 1 MHz T_A = 25°C

Notes:
* V_{IH} Min = V_{CC} -1.0V, V_{IL} Max = 0.8V (all output terminals are at no load.)
V_{CC} = 5.0V

AC CHARACTERISTICS
Z180 MPU Timing

Figures 60-68 show the timing for the Z181 MPU and the referenced parameters appear in Table A.

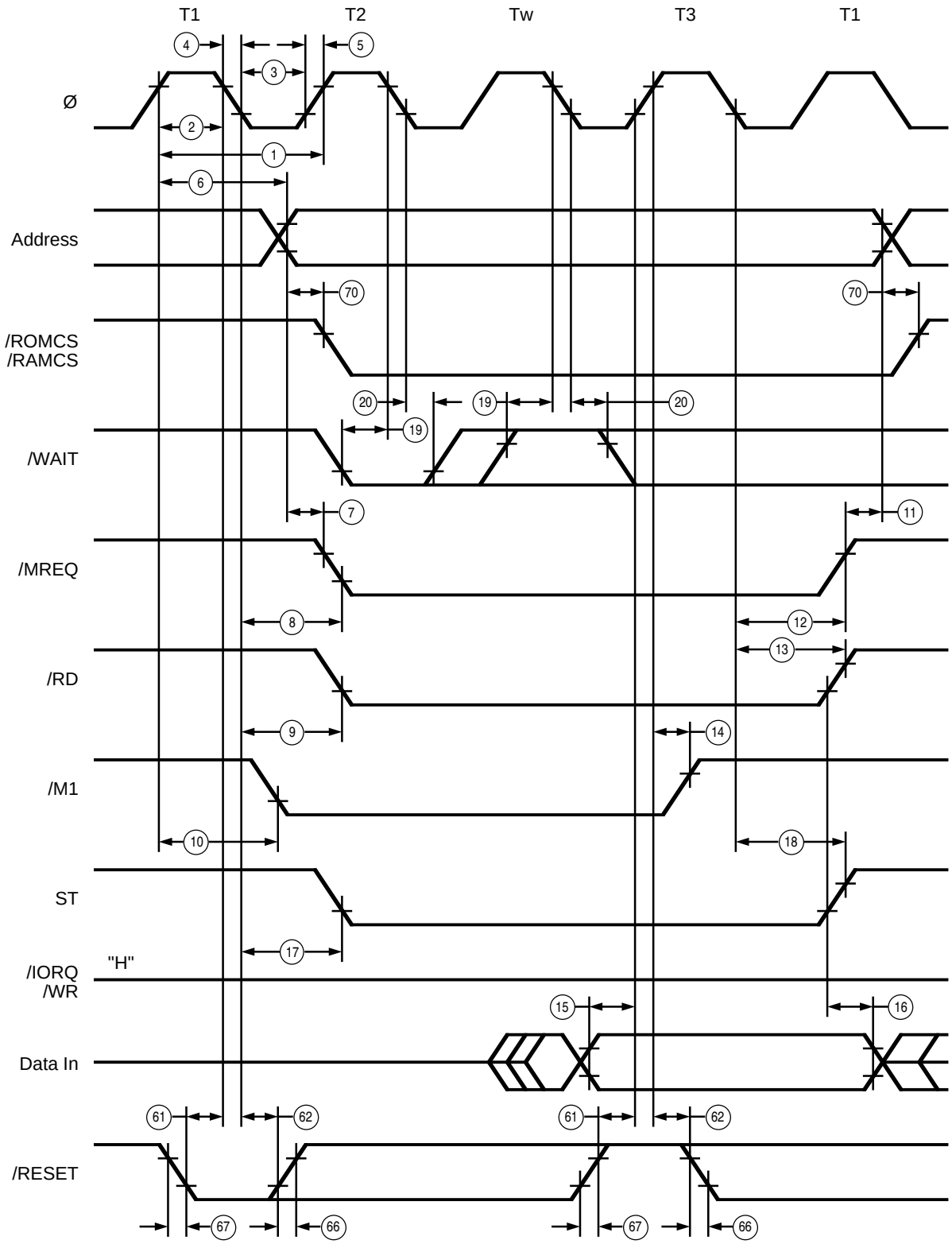
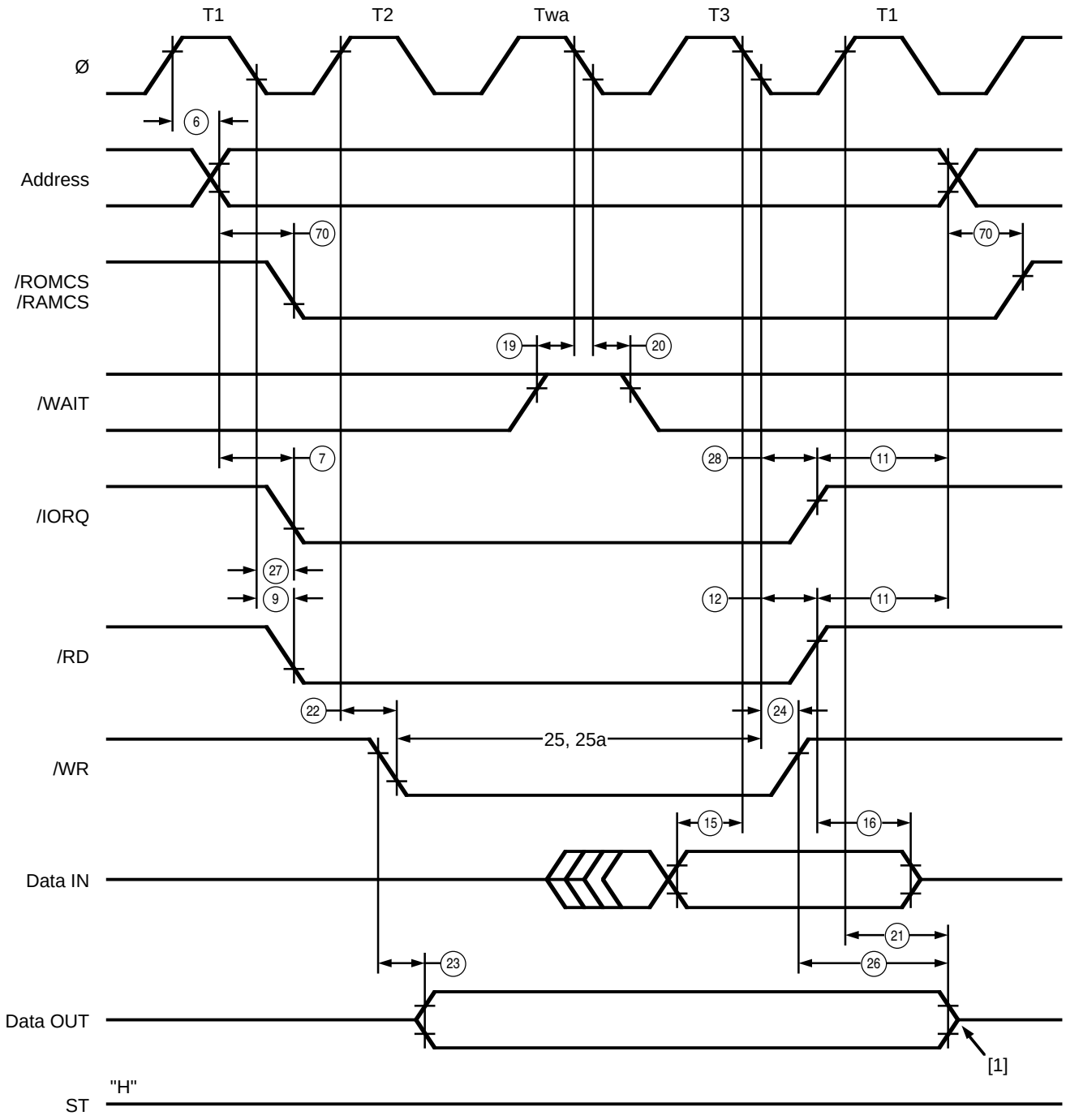


Figure 60a. Opcode Fetch Cycle

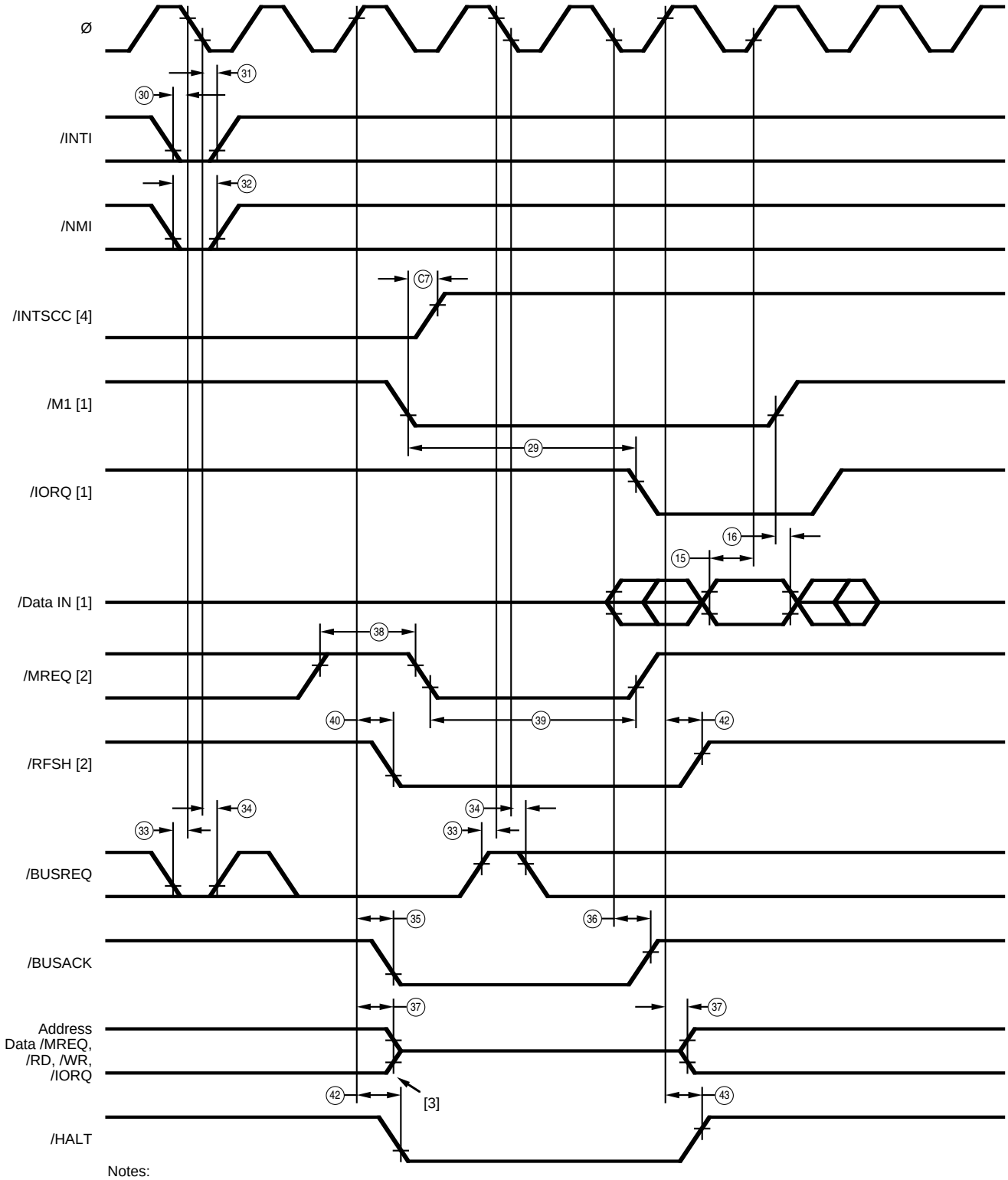


[1] Output buffer is off at this point.
[2] Memory Read/Write cycle timing is the same as this figure, except there is no automatic wait status (Twa), and /MREQ is active instead of /IORQ.

Figure 60b. I/O Read/Write, Memory Read/Write Timing

AC CHARACTERISTICS (Continued)

Z180 MPU Timing



Notes:
[1] During /INT0 acknowledge cycle
[2] During refresh cycle
[3] Output buffer is off at this point
[4] Refer to Table C, parameter 7

Figure 61. CPU Timing
(/INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode
HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

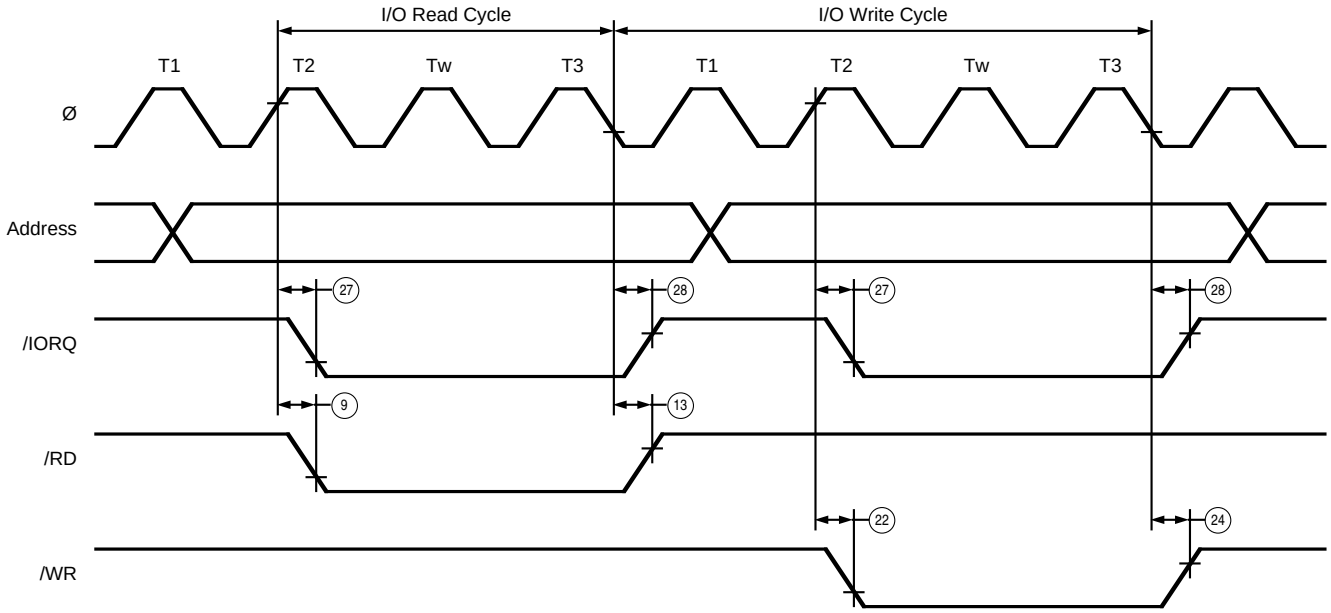
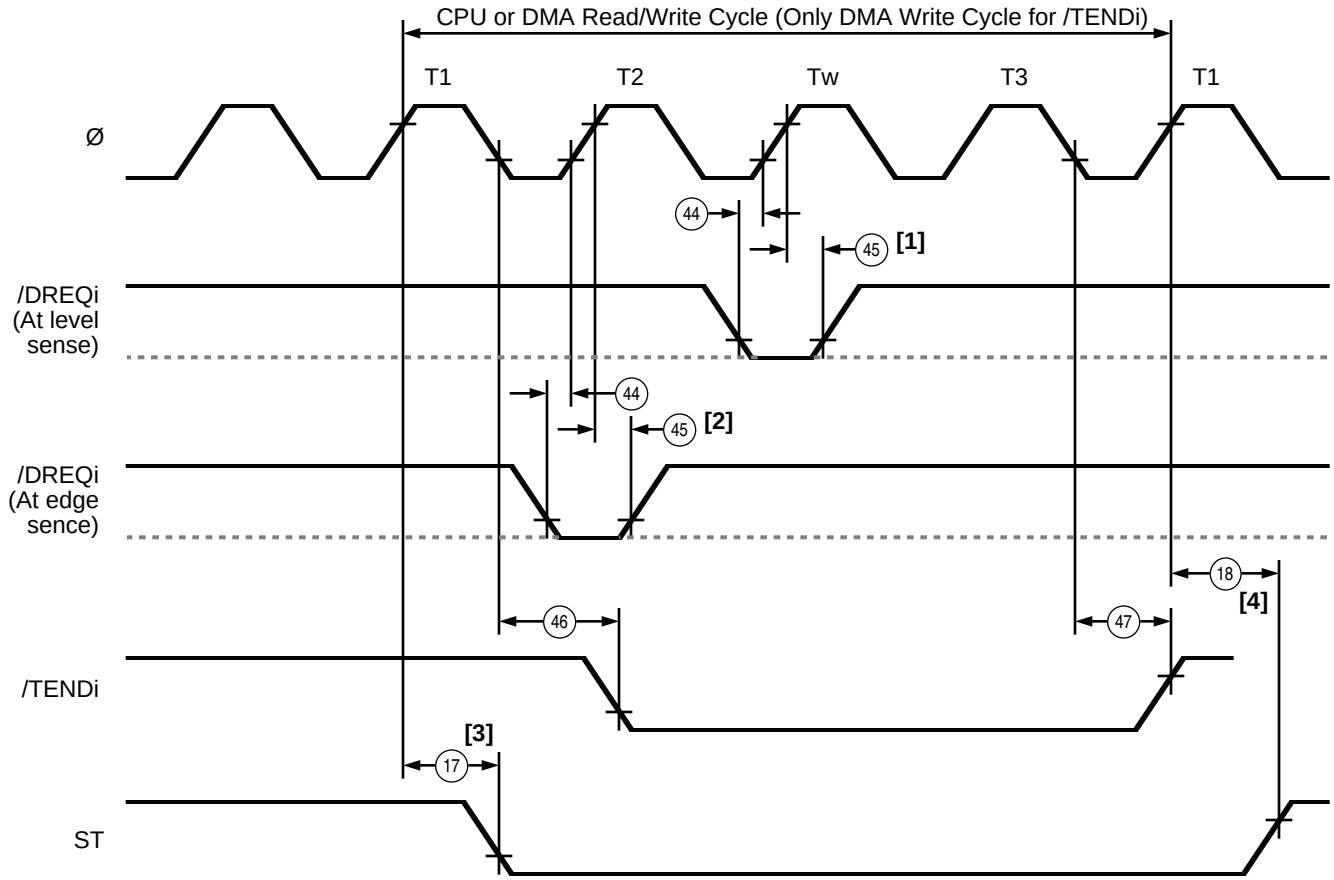


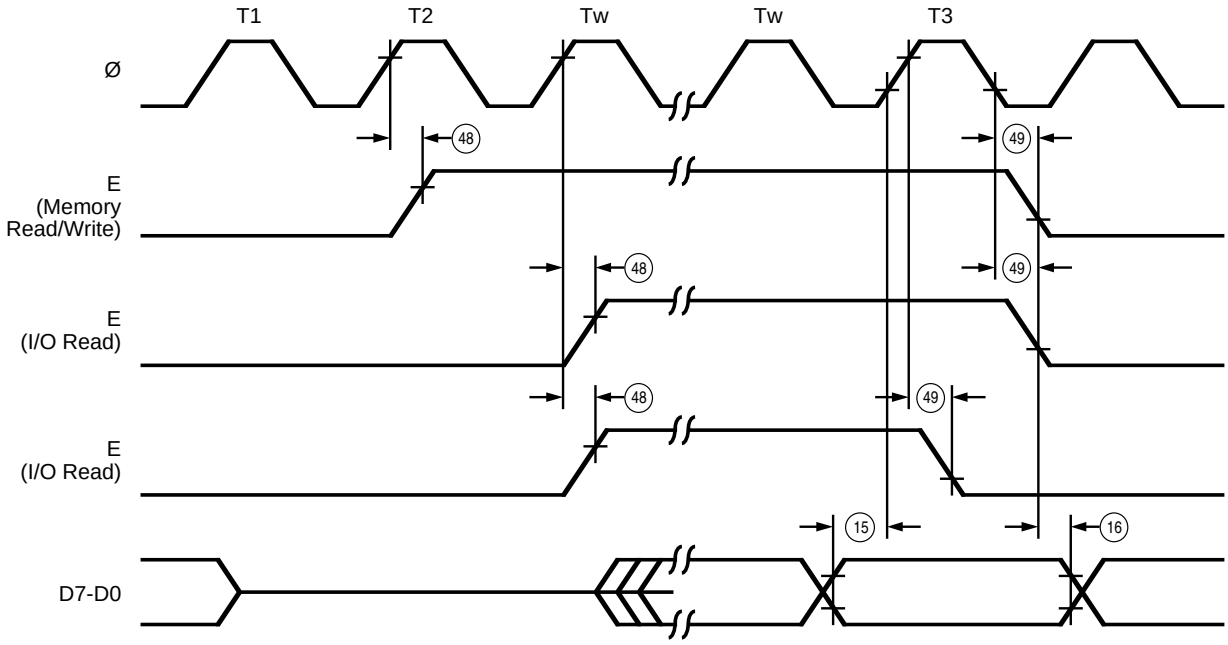
Figure 62. CPU Timing (/IOC = 0)
(I/O Read Cycle, I/O Write Cycle)

AC CHARACTERISTICS (Continued)
Z180 MPU Timing

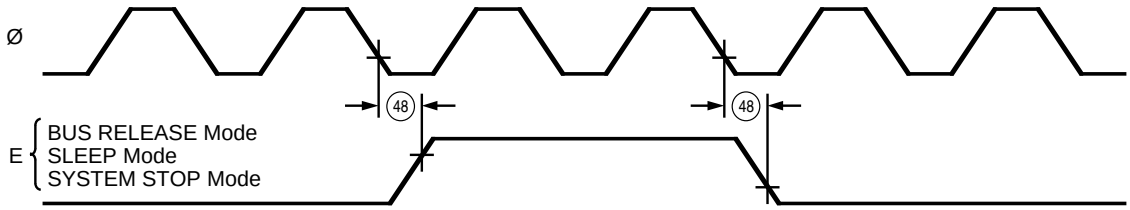


DMA Control Signals
[1] tDRQS and tDRQH are specified for the rising edge of clock followed by T3.
[2] tDRQS and tDRQH are specified for the rising edge of clock.
[3] DMA cycle starts.
[4] CPU cycle starts.

Figure 63. DMA Control Signals



(a) E Clock Timing
(Memory Read/Write Cycle, I/O Read/Write Cycle)



(b) E Clock Timing
(BUS RELEASE Mode, SLEEP Mode, SYSTEM STOP Mode)

Figure 64. E Clock Timing

AC CHARACTERISTICS (Continued)
Z180 MPU Timing

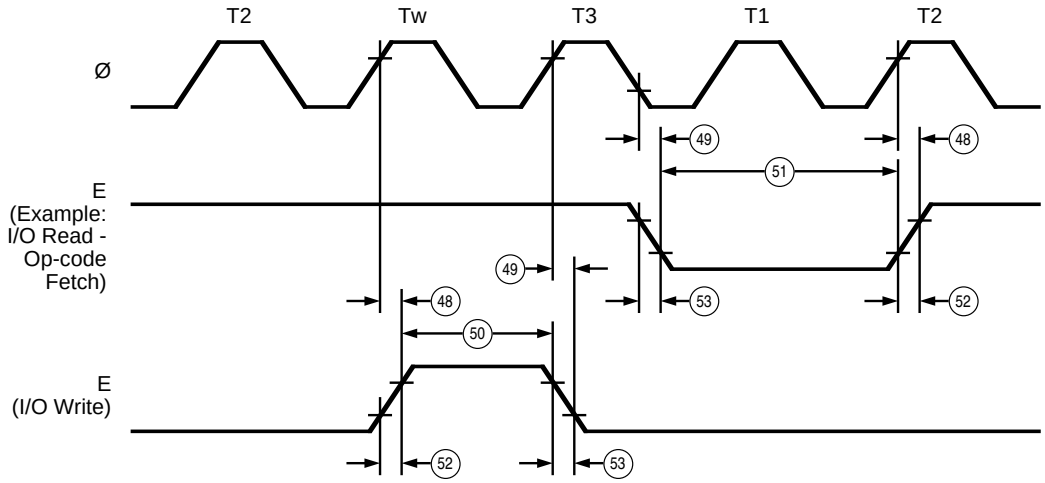


Figure 65. E Clock Timing
(Minimum timing example of PWEL and PWEH)

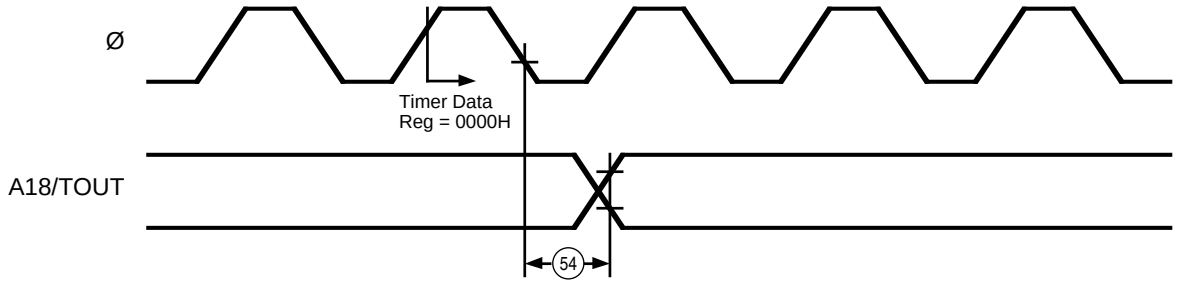


Figure 66. Timer Output Timing

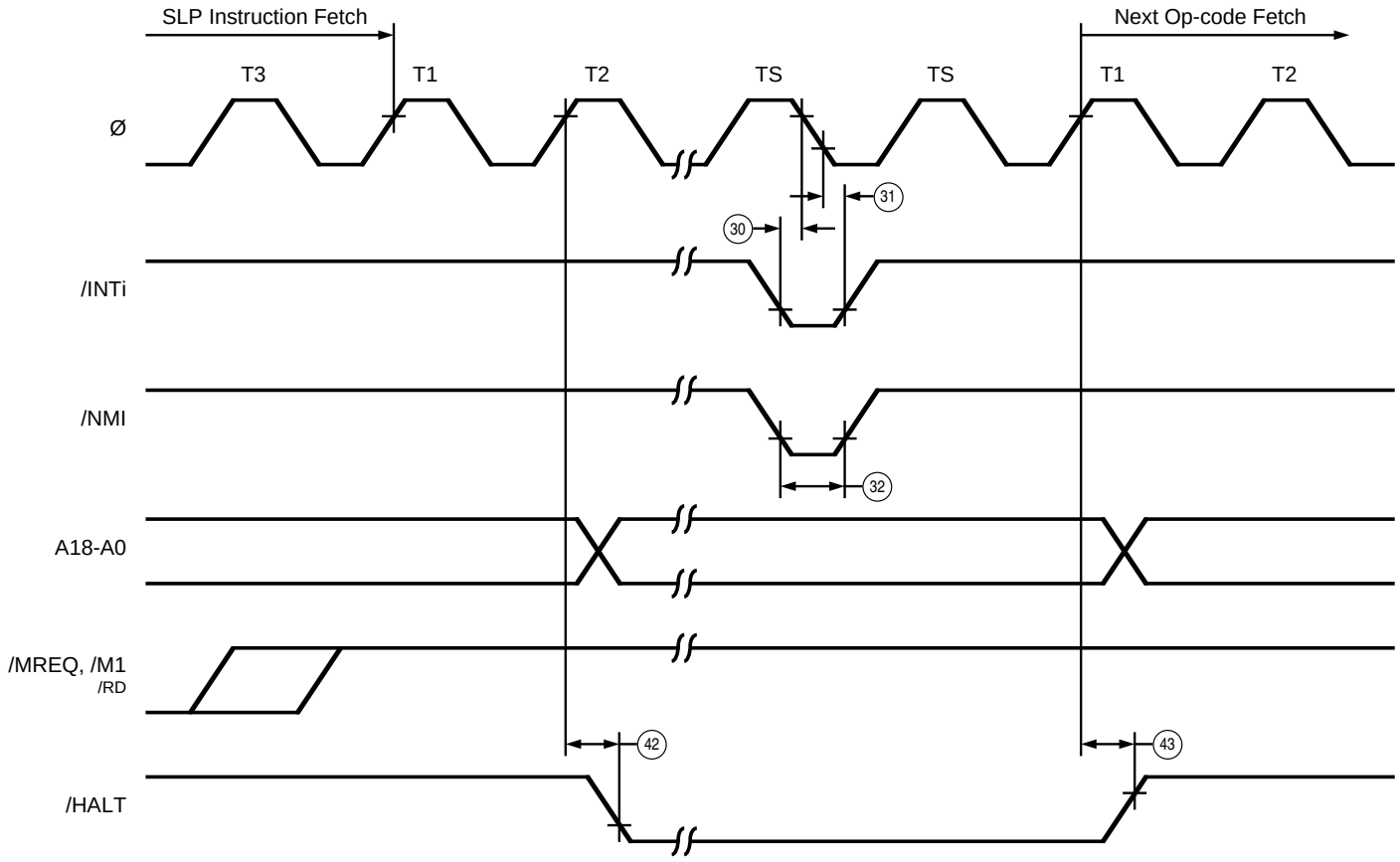


Figure 67. SLP Execution Cycle

AC CHARACTERISTICS (Continued)
Z180 MPU Timing

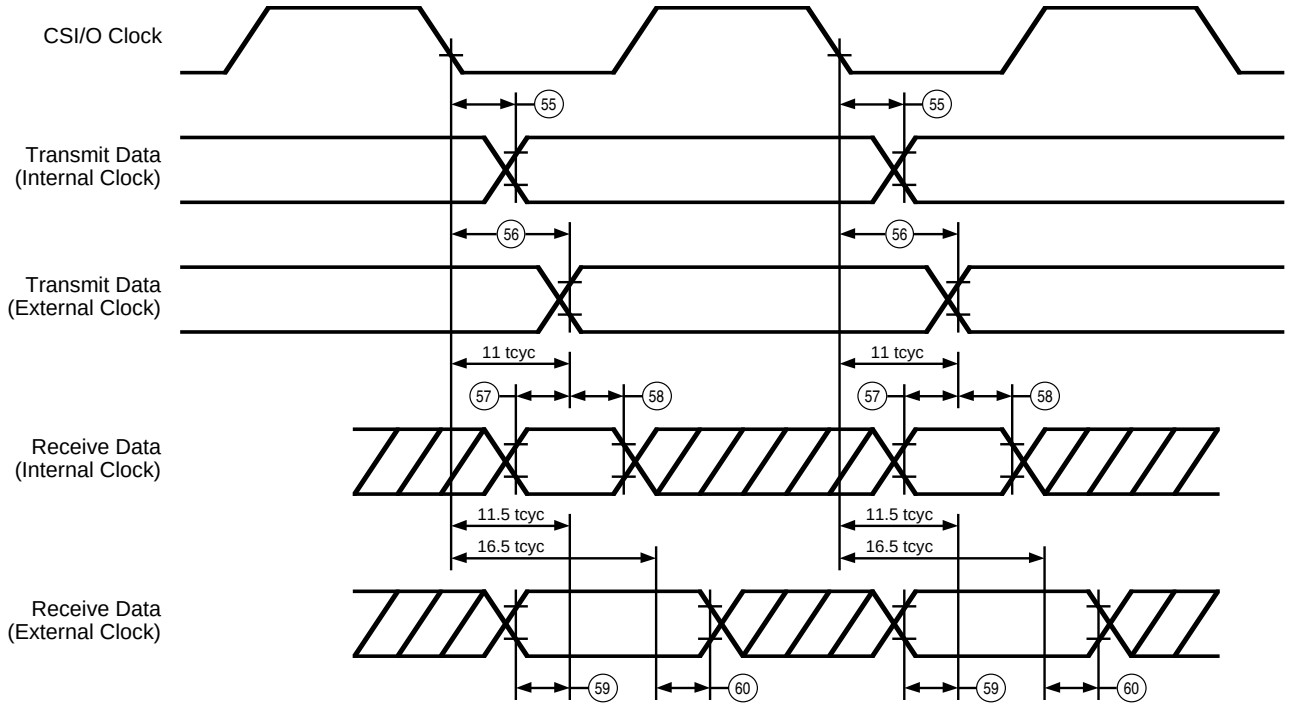


Figure 68. CSI/O Receive/Transmit Timing

Table A. Z180 CPU & 180 Peripherals Timing

No	Symbol	Parameter	Z8018110 Min	Z8018110 Max	Unit
1	tcyc	Clock Cycle Time	100	2000	ns
2	tCHW	Clock Pulse Width (High)	40		ns
3	tCLW	Clock Pulse Width (Low)	40		ns
4	tcf	Clock Fall Time		10	ns
5	tcr	Clock Rise Time		10	ns
6	tAD	Address Valid from Clock Rise		70	ns
7	tAS	Address Valid to /MREQ, /IORQ Fall	10		ns
8	tMED1	Clock Fall to /MREQ Fall Delay		50	ns
9	tRDD1	Clock Fall to /RD Fall (/IOC=1)		50	ns
		Clock Rise to /RD Fall (/IOC=0)		55	ns
10	tM1D1	Clock Rise to /M1 Fall Delay		60	ns

Table A. Z180 CPU & 180 Peripherals Timing (Continued)

No	Symbol	Parameter	Z8018110 Min	Z8018110 Max	Unit
11	tAH	Address Hold Time (/MREQ, /IORQ, /RD, /WR)	10		ns
12	tMED2	Clock Fall to /MREQ Rise Delay		50	ns
13	tRDD2	Clock Fall to /RD Rise Delay		50	ns
14	tM1D2	Clock Rise to /M1 Rise Delay		60	ns
15	tDRS	Data Read Setup Time	25		ns
16	tDRH	Data Read Hold Time	0		ns
17	tSTD1	Clock Fall to ST Fall		60	ns
18	tSTD2	Clock Fall to ST Rise		60	ns
19	tWS	/WAIT Setup Time to Clock Fall	30		ns
20	tWH	/WAIT Hold time from Clock Fall	30		ns
21	tWDZ	Clock Rise to Data Float Delay		60	ns
22	tWRD1	Clock Rise to /WR Fall Delay		50	ns
23	tWDO	/WR fall to Data Out Delay		10	ns
24	tWRD2	Clock Fall to /WR Rise		50	ns
25	tWRP	/WR Pulse Width (Memory Write Cycles)	110		ns
25a		/WR Pulse Width (I/O Write Cycles)	210		ns
26	tWDH	Write Data Hold Time from /WR Rise	10		ns
27	tIOD1	Clock Fall to /IORQ Fall Delay (/IOC=1)		50	ns
		Clock Rise to /IORQ Fall Delay (/IOC=0)		55	ns
28	tIOD2	Clock Fall /IOQR Rise Delay		50	ns
29	tIOD3	/M1 Fall to /IORQ Fall Delay	200		ns
30	tINTS	/INT Setup Time to Clock Fall	30		ns
31	tINTH	/INT Hold Time from Clock Fall	30		ns
32	tNMIW	/NMI Pulse Width	80		ns
33	tBRS	/BUSREQ Setup Time to Clock Fall	30		ns
34	tBRH	/BUSREQ Hold Time from Clock Fall	30		ns
35	tBAD1	Clock Rise to /BUSACK Fall Delay		60	ns
36	tBAD2	Clock Fall to /BUSACK Rise Delay		60	ns
37	tBZD	Clock Rise to Bus Floating Delay Time		80	ns
38	tMEWH	/MREQ Pulse Width (High)	70		ns
39	tMEWL	/MREQ Pulse Width (Low)	80		ns
40	tRFD1	Clock Rise to /RFSH Fall Delay		60	ns
41	tRFD2	Clock Rise to /RFSH Rise Delay		60	ns
42	tHAD1	Clock Rise to /HALT Fall Delay		50	ns
43	tHAD2	Clock Rise to /HALT Rise Delay		50	ns
44	tDRQS	/DREQi Setup Time to Clock Rise	30		ns
45	tDRQH	/DREQi Hold Time from Clock Rise	30		ns
46	tTED1	Clock Fall to /TENDi Fall Delay		50	ns

AC CHARACTERISTICS (Continued)
Z180™ MPU Timing

Table A. Z180 CPU &180 Peripherals Timing (Continued)

No	Symbol	Parameter	Z8018110 Min	Z8018110 Max	Unit
47	tTED2	Clock Fall to /TENDi Rise Delay		50	ns
48	tED1	Clock Rise to E Rise Delay		60	ns
49	tED2	Clock Edge to E Fall Delay		60	ns
50	PWEH	E Pulse Width (High)	55		ns
51	PWEL	E Pulse Width (Low)	110		ns
52	tEr	Enable Rise Time		20	ns
53	tEf	Enable Fall Time		20	ns
54	tTOD	Clock Fall to Timer Output Delay		150	ns
55	tSTDI	CSI/O Tx Data Delay Time (Internal Clock Operation)		150	ns
56	tSTDE	CSI/O Tx Data Delay Time (External Clock Operation)		7.5tcyc+150	ns
57	tSRSI	CSI/O Rx Data Setup Time (Internal Clock Operation)	1		tcyc
58	tSRHI	CSI/O Rx Data Hold Time (Internal Clock Operation)	1		tcyc
59	tSRSE	CSI/O Rx Data Setup Time (External Clock Operation)	1		tcyc
60	tSRHE	CSI/O Rx Data Hold Time (External Clock Operation)	1		tcyc
61	tRES	/RESET Setup Time to Clock Fall	80		ns
62	tREH	/RESET Hold Time from Clock Fall	50		ns
63	tOSC	Oscillator Stabilization Time		20	ms
64	tEXr	External Clock Rise Time (EXTAL)		25	ns
65	tEXf	External Clock Fall Time (EXTAL)		25	ns
66	tRr	/RESET Rise Time		50	ns
67	tRf	/RESET Fall Time		50	ns
68	tIr	Input Rise Time (Except EXTAL, /RESET)		100	ns
69	tIf	Input Fall Time (Except EXTAL, /RESET)		100	ns
70	TdCS(A)	Address Valid to /ROMCS, /RAMCS Valid Delay		20	ns

AC CHARACTERISTICS (Continued)
CTC Timing

Figure 69 shows the timing for the on-chip CTC. Parameters referenced in this figure appear in Table B.

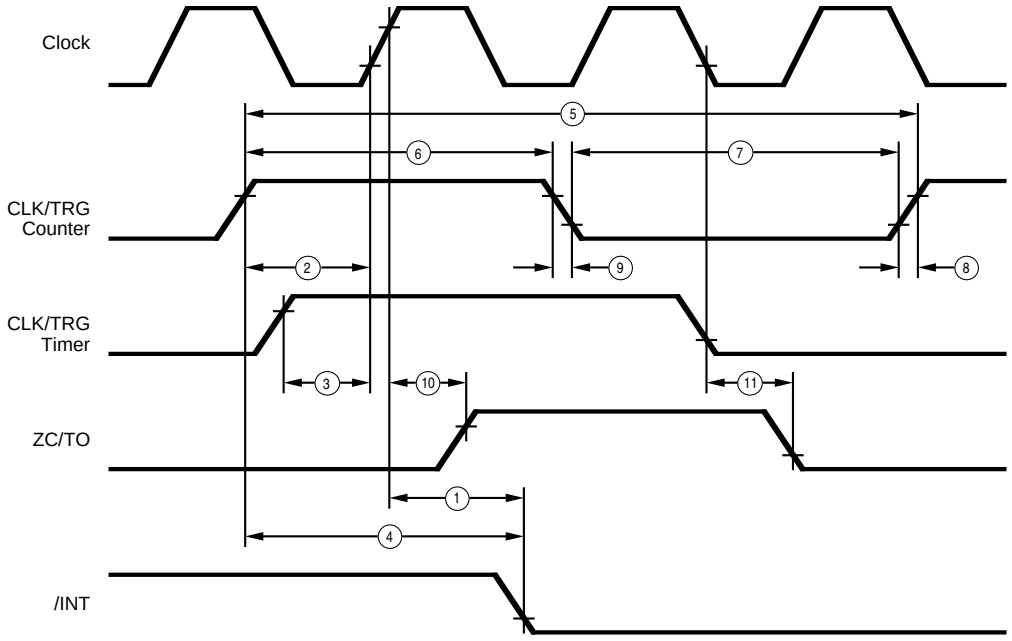


Figure 69. CTC Timing

Table B. CTC Timing Parameters

No	Symbol	Parameter	Z8018110 Min	Z8018110 Max	Unit	Note
1	TdCr(INTf)	Clock Rise to /INT Fall Delay		(TcC+100)	ns	[B1]
2	TsCTRr(Cr)c	CLK/TRG Rise to Clock Rise Setup Time for Immediate Count	90		ns	[B2]
3	TsCTR(Ct)	CLK/TRG Rise to Clock Rise Setup Time for Enabling of Prescaler On Following Clock Rise		90	ns	[B1]
4	TdCTRr(INTf)	CLK/TRG Rise to /INT Fall Delay				
		TsCTR(C) Satisfied		(1)+(3)	ns	[B2]
		TsCTR(C) Not Satisfied		TcC+(1)+(3)	ns	[B2]
5	TcCTR	CLK/TRG Cycle Time	(2TcC)	DC	ns	[B3]
6	TwCTRh	CLK/TRG Width (Low)	90	DC	ns	
7	TwCTRl	CLK/TRG Width (High)	90	DC	ns	
8	TrCTR	CLK/TRG Rise Time		30	ns	
9	TfCTR	CLK/TRG Fall Time		30	ns	
10	TdCr(ZCr)	Clock Rise to ZC/TO Rise Delay		80	ns	
11	TdCf(ZCf)	Clock Fall to ZC/TO Fall Delay		80	ns	

Notes for Table B:
[B1] Timer Mode
[B2] Counter Mode
[B3] Counter Mode Only. When using a cycle time less than 3TcC, parameter #2 must be met.

AC CHARACTERISTICS (Continued)
SCC Timing

Figure 70 shows the AC characteristics for the on-chip SCC. Parameters referenced in this figure appear in Table C.

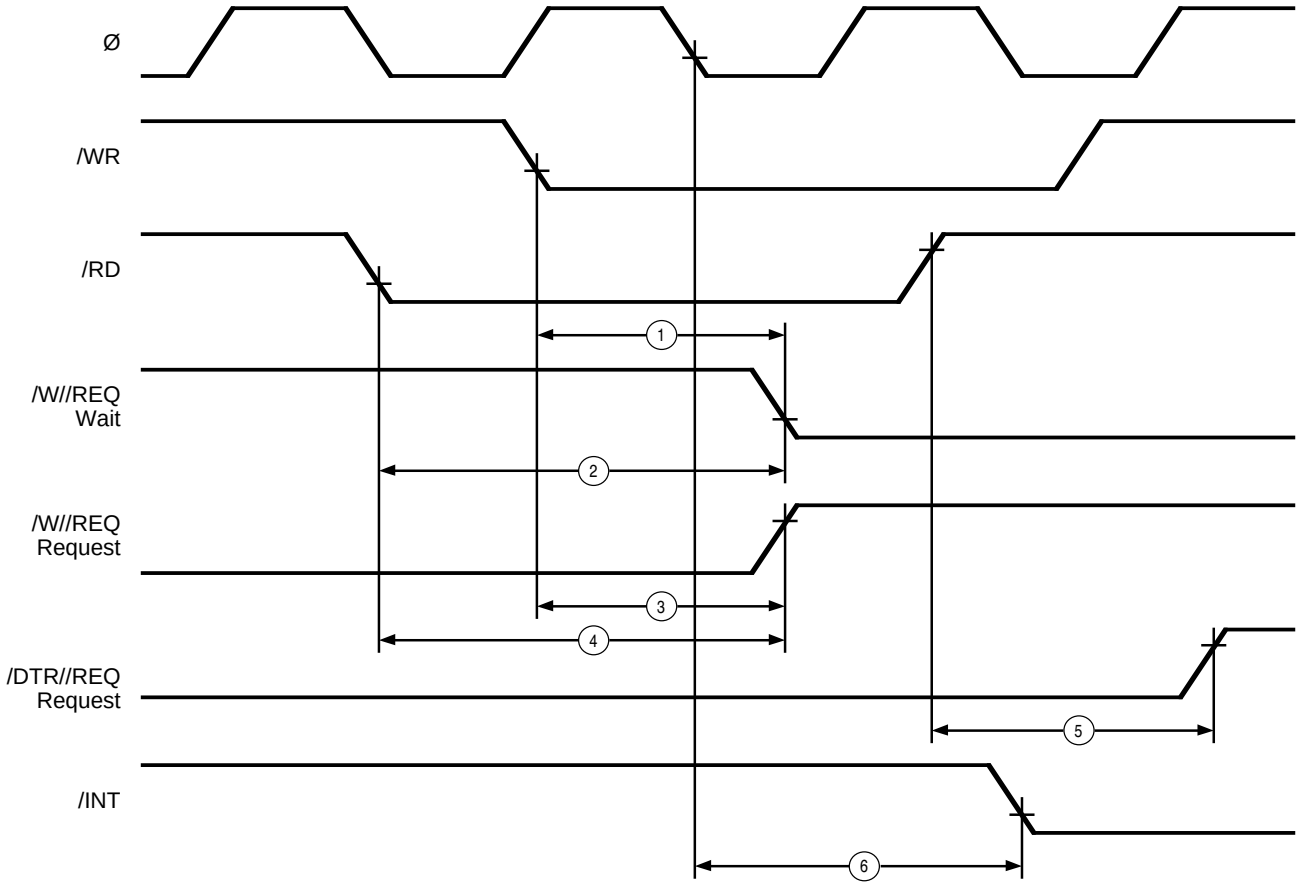


Figure 70. SCC AC Parameters

Table C. SCC Timing Parameters (85C30 AC Characteristics)

No	Symbol	Parameter	Z8018110 Min	Z8018110 Max	Unit	Note
1	TdWR(W)	/WR Fall to Wait Valid Delay		180 + TcC	ns	[C1]
2	TdWR(W)	/RD Fall to Wait Valid Delay		180	ns	[C1]
3	TdWRf(REQ)	/WR Fall to /W//REQ Not Valid Delay		180 + TcC	ns	
4	TdRDf(REQ)	/RD Fall to /W//REQ Not Valid Delay		180	ns	
5	TdWRr(REQ)	/WR Rise to /DTR//REQ Not Valid Delay		5TcC	ns	
6	TdPC(INT)	Clock to /INT Valid Delay		500	ns	[C1]
7	TdRDA(INT)	/M1 Fall to /INT Inactive Delay		TBS	ns	[C1]

Note for Table C:
[C1] Open-drain output, measured with open-drain test load.

Figure 71 shows the general timing for the on-chip SCC. Parameters referenced in this figure appear in Table D.

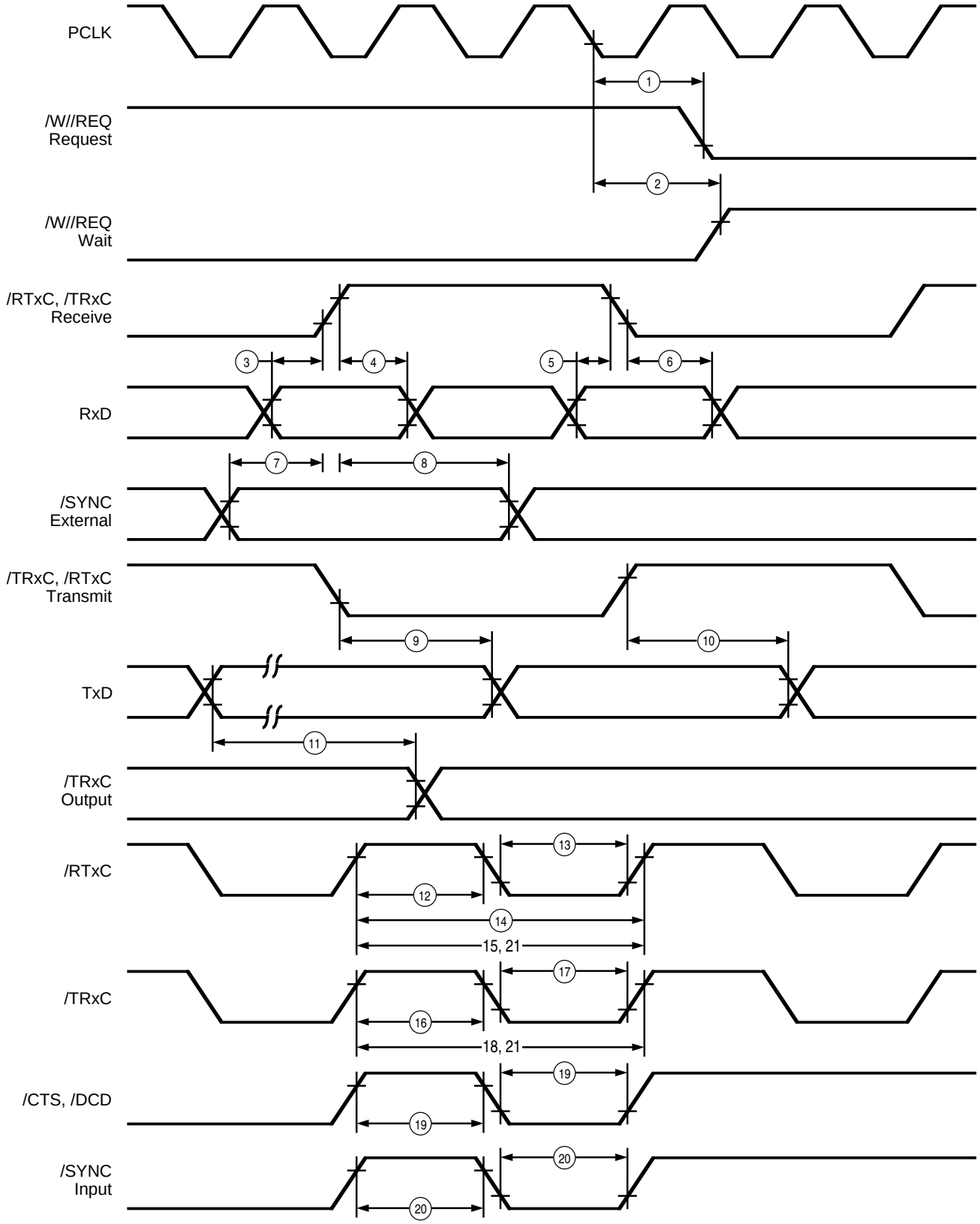


Figure 71. SCC General Timing

AC CHARACTERISTICS (Continued)
SCC General Timing

Table D. SCC General Timing Parameters

No	Symbol	Parameter	Z8018110 Min	Z8018110 Max	Unit	Note
1	TdPC(REQ)	Clock Fall to /W//REQ Valid		200	ns	
2	TdPC(W)	Clock Fall to Wait Inactive		300	ns	
3	TsRXD(RXCr)	RxD to /RxC Rise Setup Time	0		ns	[D1]
4	ThRXD(RXCr)	RxD to /RxC Rise Hold Time	125		ns	[D1]
5	TsRXD(RXCf)	RxD to /RxC Fall Setup Time	0		ns	[D1,4]
6	ThRXD(RXCf)	RxD to /RxC Fall Hold Time	125		ns	[D1,4]
7	TsSY(RXC)	/SYNC to /RxC Setup Time	–150		ns	[D1]
8	ThSY(RXC)	/SYNC to /RxC Hold Time	5TcC		ns	[D1]
9	TdTXCf(TXD)	/TxC Fall to TxD Delay		150	ns	[D2]
10	TdTXCr(TXD)	/TxC Rise to TxD Delay		150	ns	[D2,4]
11	TdTXD(TRX)	TxD to /TRxC Delay		140	ns	
12	TwRTXh	/RTxC High Width	120		ns	[D5]
13	TwRTXl	/RTxC Low Width	120		ns	[D5]
14	TcRTX	/RTxC Cycle Time (RxD, TxD)	400		ns	[D5,6]
15	TcRTXX	Xtal OSC Period	100	1000	ns	[D3]
16	TwTRXh	/TRxC High Width	120		ns	[D5]
17	TwTRXl	/TRxC Low Width	120		ns	[D5]
18	TcTRX	/TRxC Cycle Time	400		ns	[D5,7]
19	TwEXT	/DCD or /CTS Pulse Width	120		ns	
20	TwSY	/SYNC Pulse Width	100		ns	
21	TxRx(DPLL)	DPLL Cycle Time	50		ns	[D6,7]

Notes to Table D:
[D1] /RXC is /RTxC or /TRxC, whichever is supplying the receiver clock.
[D2] /TXC is /TRxC or /RTxC, whichever is supplying the transmitter clock.
[D3] Both /RTxC and /SYNC pins have 30 pF Capacitors (to Ground).
[D4] Parameter applies only to FM encoding/decoding.
[D5] Parameter applies only to transmitter and receiver; baud rate generator timing requirements are different.
[D6] The maximum receive or transmit data rate is 1/4 TcC.
[D7] Applies to DPLL clock source only; maximum data rate of 1/4 TcC still applies.

Figure 72 shows the system timing for the on-chip SCC. Parameters referenced in this figure appear in Table E.

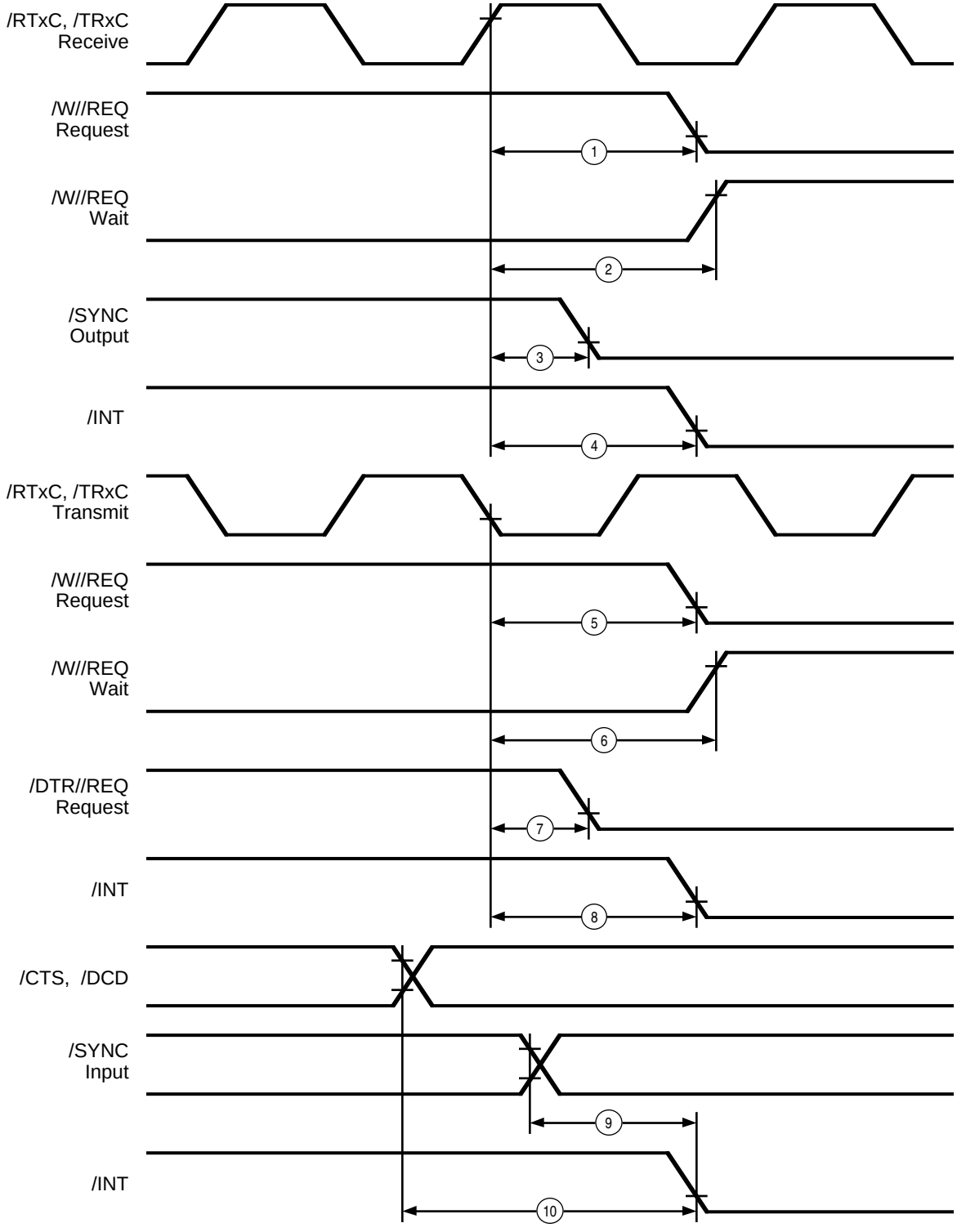


Figure 72. SCC System Timing

AC CHARACTERISTICS (Continued)
SCC System Timing

Table E. SCC System Timing Parameters

No	Symbol	Parameter	Z8018110 Min	Z8018110 Max	Unit	Note
1	TdRxC(REQ)	/RxC to /W//REQ Valid	8	12	TcC	[E2]
2	TdRxC(W)	/RxC to Wait inactive	8	14	TcC	[E1,2]
3	TdRxC(SY)	/RxC to /SYNC Valid	4	7	TcC	[E2]
4	TdRxC(INT)	/RxC to /INT Valid	10	16	TcC	[E1,2]
5	TdTxC(REQ)	/TxC to /W//REQ Valid	5	8	TcC	[E3]
6	TdTxC(W)	/TxC to Wait inactive	5	11	TcC	[E1,3]
7	TdRxC(DRQ)	/TxC to /DTR//REQ Valid	4	7	TcC	[E3]
8	TdTxC(INT)	/TxC to /INT Valid	6	10	TcC	[E1,3]
9	TdSY(INT)	/SYNC to /INT Valid	2	6	TcC	[E1]
10	TdEXT(INT)	/DCD or /CTS to /INT Valid	2	6	TcC	[E1]

Notes for Table E:
[E1] Open-drain output, measured with open-drain test load.
[E2] /RXC is /RTxC or /TRxC, whichever is supplying the receiver clock.
[E3] /TXC is /TRxC or /RTxC, whichever is supplying the transmitter clock.

AC CHARACTERISTICS (Continued)
PIA General-Purpose I/O Port Timing

Figure 73 shows the timing for the PIA ports. Parameters referenced in this figure appear in Table F.

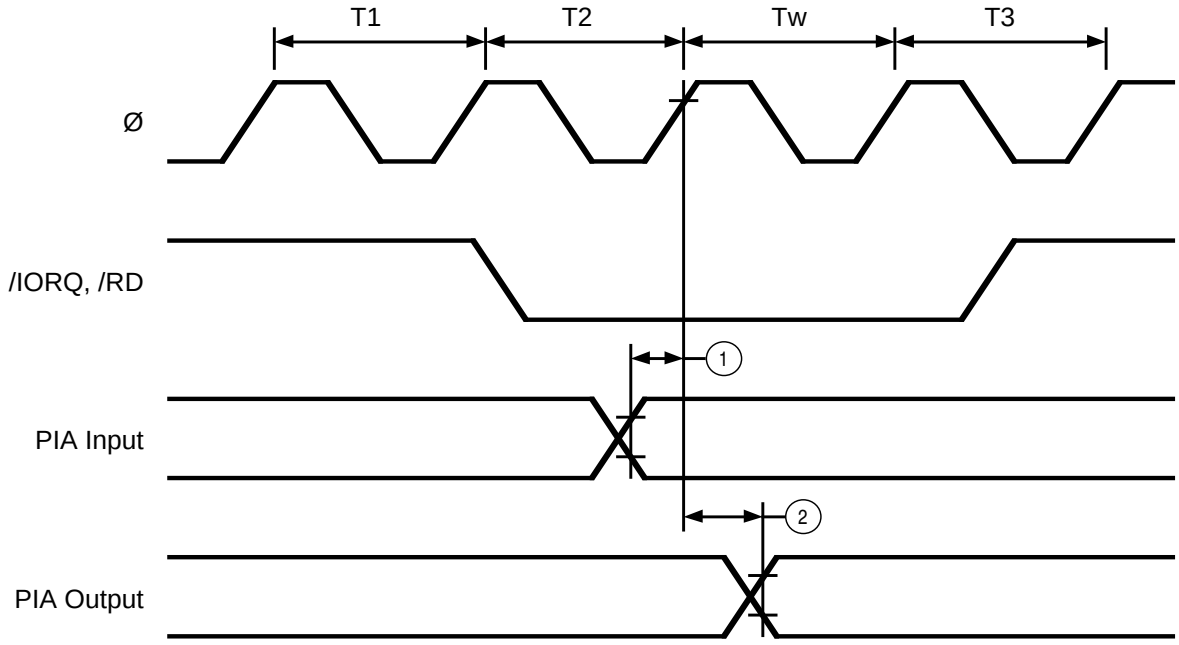


Figure 73. PIA Timing

Table F. PIA General-Purpose I/O Timing Parameters

No	Symbol	Parameter	Z8018110 Min	Z8018110 Max	Unit
1	TsPIA(C)	PIA Data Setup time to Clock Rise	10		ns
2	TdCr(PIA)	Clock Rise to PIA Data Valid Delay		50	ns

AC CHARACTERISTICS (Continued)
Interrupt Daisy-Chain Timing

Figure 74 shows the interrupt daisy-chain timing. Parameters referenced in this figure appear in Table G.

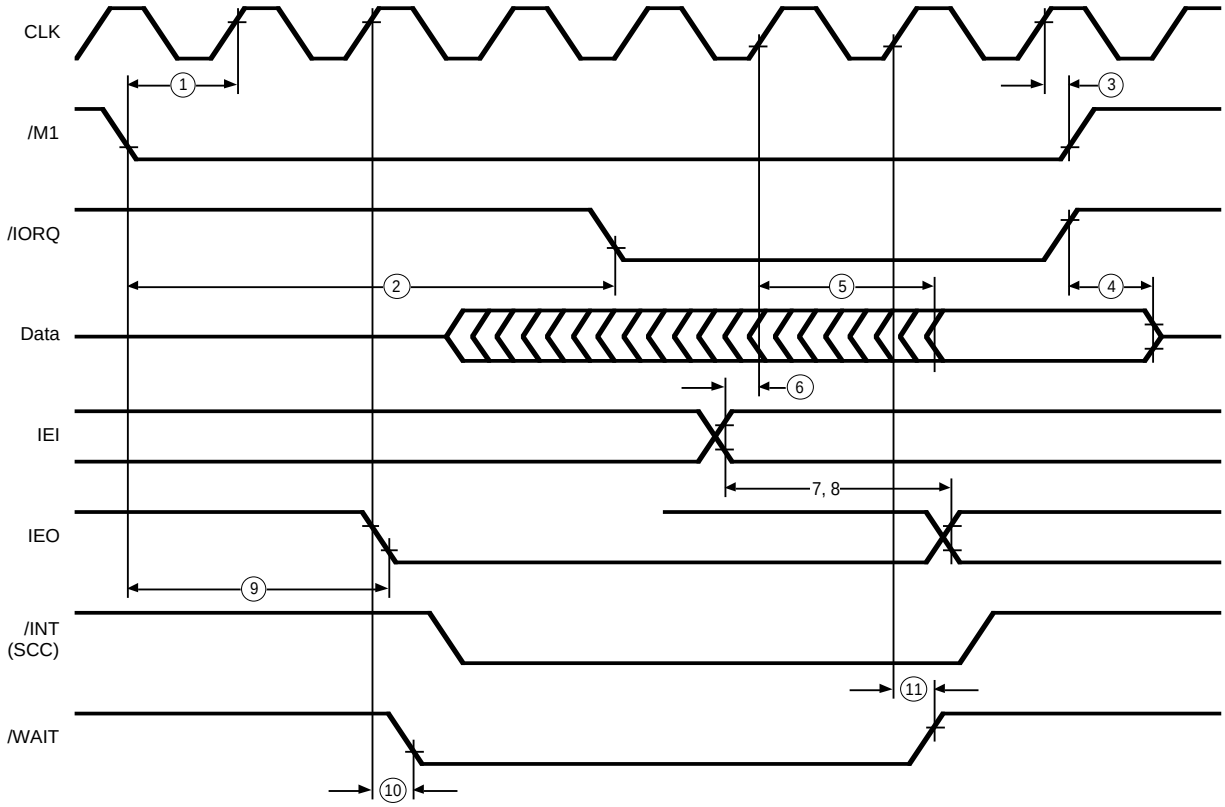


Figure 74. Interrupt Daisy-Chain Timing

Table G. Interrupt Daisy-Chain Timing Parameters

No	Symbol	Parameter	Z8018110 Min	Z8018110 Max	Unit
1	TsM1(Cr)	/M1 Fall to Clock Rise Setup Time	20		ns
2	TsM1(IO)INTA	/M1 Fall to /IORQ Fall Setup Time (During INTACK Cycle)	2TcC		ns
3	Th	Hold Time	0		
4	TdM1r(DOz)	/M1 Rise to Data Out Float Delay	0		ns
5	TdCr(DO)	Clock Rise to Data Out Delay			
6	TsIEI(TW4)	IEI to T_{W4} Rise Setup Time	95		ns
7	TdIEIf(IEOf)	IEI Fall to IEO Fall Delay			
8	TdIEIr(IEOr)	IEO Rise to IEO Rise Delay			
9	TdM1f(IEOf)	/M1 Fall to IEO Fall Delay			
10	TdCWA(f)INTA	Clock Rise to /WAIT Fall Delay			
11	TdCWA(r)INTA	Clock Rise to /WAIT Rise Delay			

Note for Interrupt Acknowledge Cycle and Daisy Chain

When using the interrupt daisy chained device(s) for other than the Z181 (without external logic), the following restrictions/notes apply:

The device(s) must be connected to the higher priority location (Figure 75).

The device(s) IEI-IEO delay must be less than two clock cycles.

The Z181 on-chip interface logic inserts another three wait states into the interrupt acknowledge cycle to meet the on-chip SCC and the Z80 CTC timing requirements. (For a total of five wait states, including the two automatically inserted wait states).

To meet the timing requirements, the Z181's on-chip circuit generates interface signals for the SCC and CTC. Figure 78 has the timing during the interrupt acknowledge cycle, including the internally generated signals.

The following are three separate cases for the daisy-chain settle times:

Case 1 - SCC: The SCC /INTACK signal goes active on the T1 clock fall time. The settle time is from SCC /INTACK active until the SCC /RD signal goes active on the fourth rising wait state clock.

Case 2 - CTC: The settle time for the on-chip /IORQ is between the fall of /M1 until the internal CTC /IORQ goes active on the rise of the fourth wait state (the same time as SCC /RD goes active).

Case 3 - OFF-chip Z80 Peripheral: The settle time for the off-chip Z80 peripheral is from the fall of /M1 until CTC /IORQ goes active. Since the Z181's external /IORQ signal goes active on the clock fall of the first automatically inserted wait state (T_{WA}), the external daisy-chain device must be connected to the upper chain location. Also, it must settle within two clock cycles.

If any peripheral is connected externally with a lower daisy chain priority than Z181 peripherals, /IORQ must be delayed by external logic as shown in Figure 79.

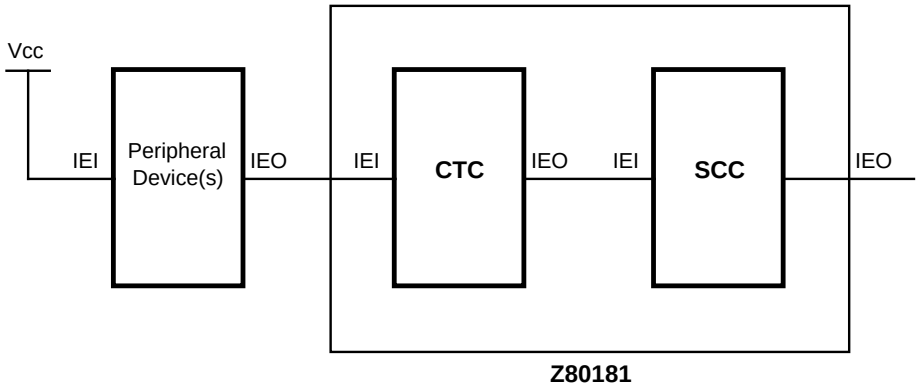


Figure 75. Peripheral Device as Part of the Daisy Chain

AC CHARACTERISTICS (Continued)
Read Write External BUS Master Timing

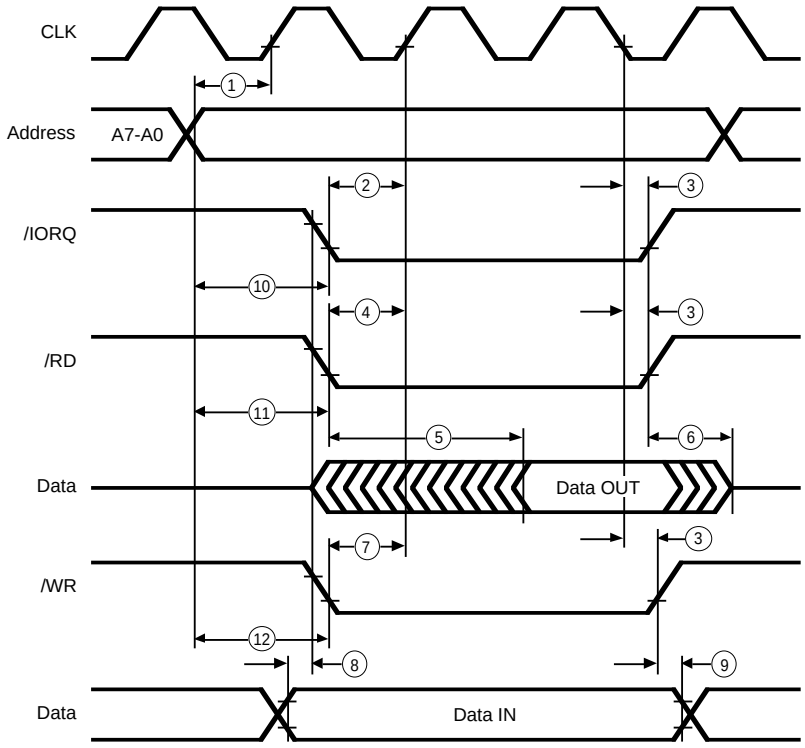


Figure 76. Read/Write External BUS Master Timing

Table H. External Bus Master Interface Timing (Read/Write Cycles)

No	Symbol	Parameter	Z8018110 Min	Z8018110 Max	Unit
1	TsA(Cr)	Address to CLK Rise Setup Time	20		ns
2	TsIO(Cr)	/IORQ Fall to CLK Rise Setup Time	20		ns
3	Th	Hold Time	0		
4	TsRD(Cr)	/RD Fall to CLK Rise Setup Time	20		ns
5	TdRD(DO)	/RD Fall to Data Out Delay		120	ns
6	TdRIr(DOz)	/RD, /IORQ Rise to Read Data Float	0		
7	TsWR(Cr)	/WR Fall to CLK Rise Setup Time	20		ns
8	TsDi(WRf)	Data in to /WR Fall Setup Time	0		
9	ThWIr(Di)	/IORQ, /WR Rise to Data In Hold Time	0		
10	TsA(IORQf)	Address to /IORQ Fall Setup Time	50		ns
11	TsA(RDf)	Address to /RD Fall Setup Time	50		ns
12	TsA(WRf)	Address to /WR Fall Setup Time	50		ns

SCC External BUS Master Timing

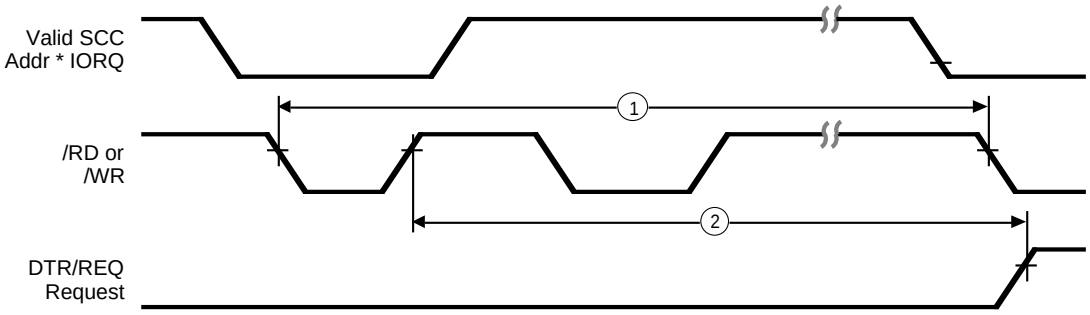


Figure 77. SCC External BUS Master Timing

Table I. External Bus Master Interface Timing (SCC Related Timing)

No	Symbol	Parameter	Z8018110 Min	Z8018110 Max	Unit	Notes
1	TrC	Valid Access Recovery Time	4TcC		ns	[1]
2	TdRDr(REQ)	/RD Rise to /DTR//REQ Not Valid Delay	4TcC		ns	

Note for Table I:
[1] Only applies between transactions involving the SCC.

AC CHARACTERISTICS (Continued)

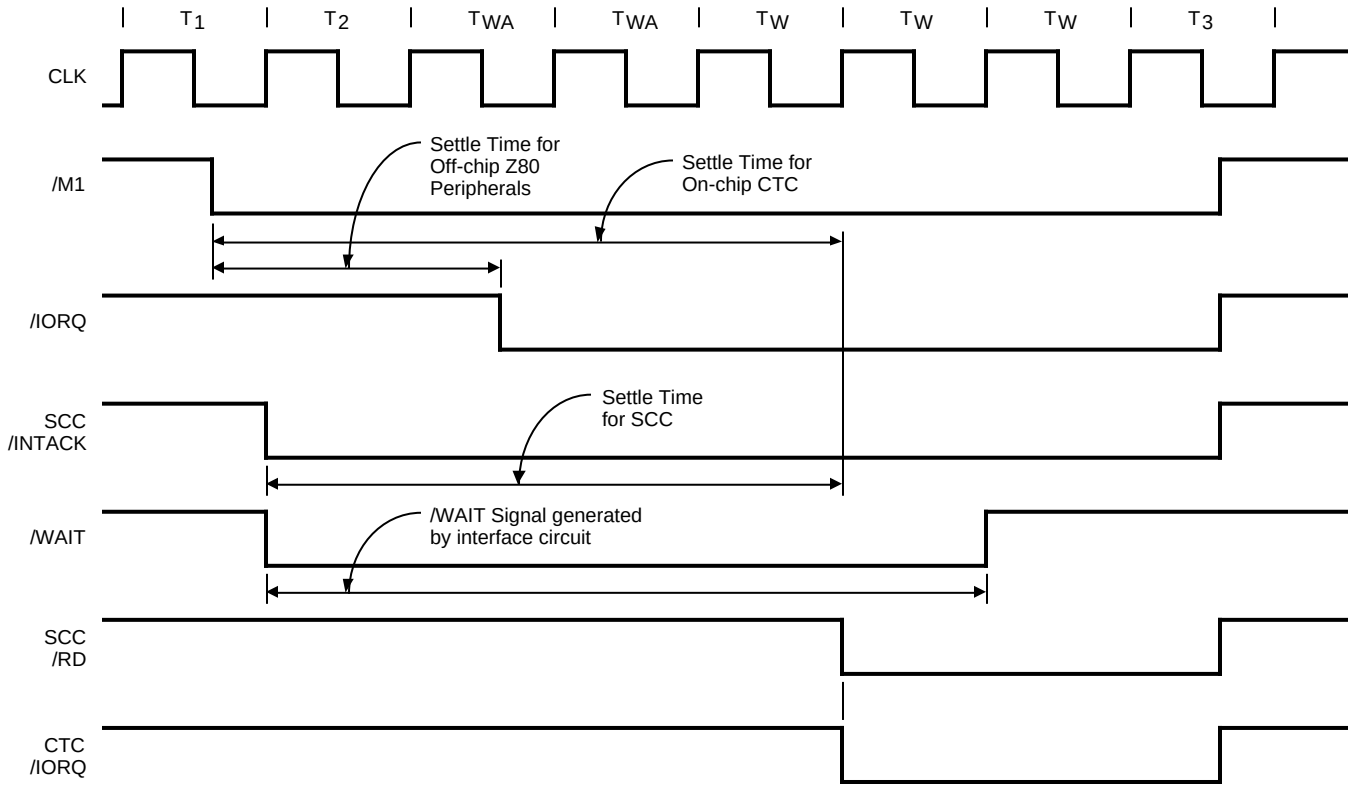


Figure 78. Interrupt Acknowledge Cycle Timing

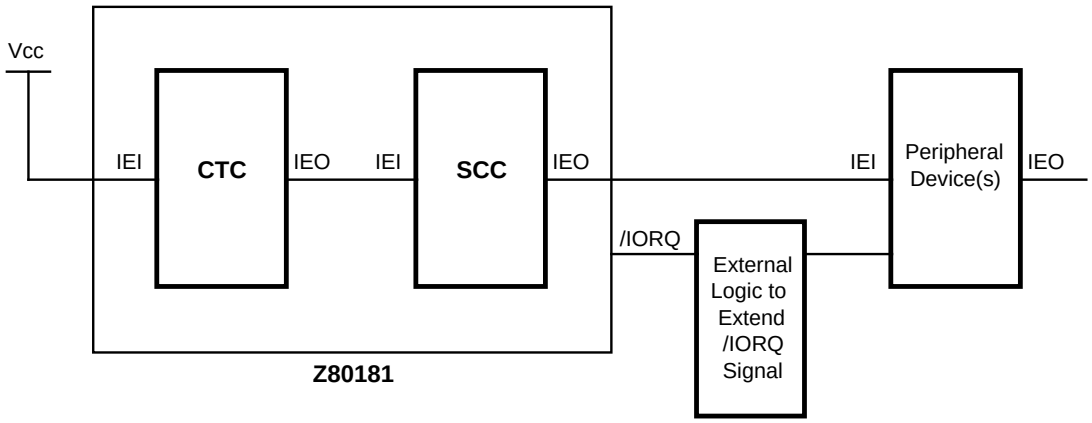
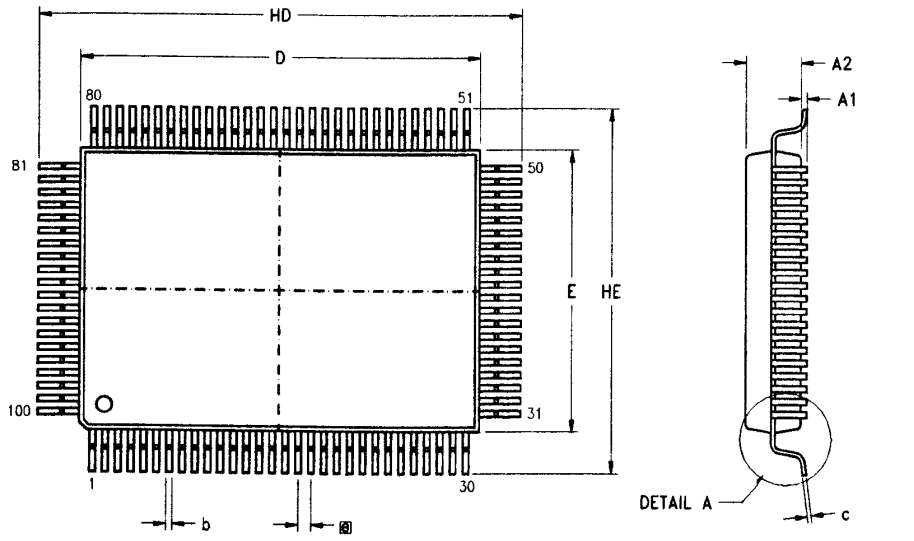
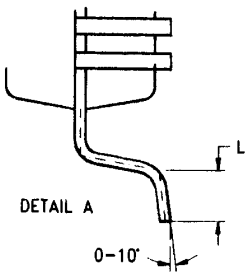


Figure 79. Peripheral Device as Part of the Daisy Chain

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	.004	.012
A2	2.60	2.80	.102	.110
b	0.25	0.40	.010	.016
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.65 TYP		.0256 TYP	
L	0.70	1.10	.028	.043



NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. MAX COPLANARITY : .10 / .004

100-Pin QFP Package Diagram

ORDERING INFORMATION

Z80181 (10 MHz)

Extended Temperature

100-Pin QFP

Z8018110FEC

Package

Longer Lead Time

F = Plastic Quad Flat Pack

Temperature

Longer Lead Time

E = –40°C to +100°C

Environmental

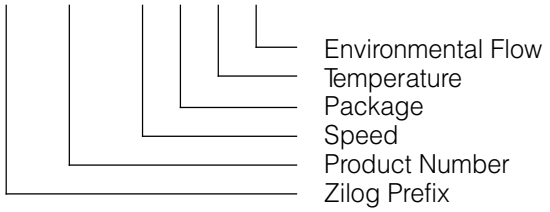
C = Plastic Standard

Speed

10 = 10 MHz

Example:

Z 80181 10 F E C is a Z80181, 10 MHz, QFP, –40°C to +100°C, Plastic Standard Flow



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