

# ZXM64N035L3

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## 35V N-CHANNEL ENHANCEMENT MODE MOSFET

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### SUMMARY

$V_{(BR)DSS} = 35V$ ;  $R_{DS(on)} = 0.060\Omega$ ;  $I_D = 13A$

### DESCRIPTION

This new generation of high cell density planar MOSFETs from Zetex utilises a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage, power management applications.

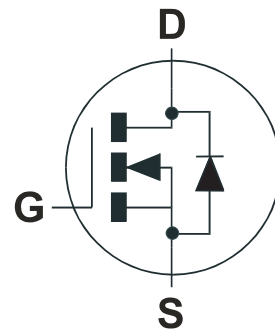


### FEATURES

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- TO220 package

### APPLICATIONS

- 100W Class D Audio Output Stage
- Motor Control

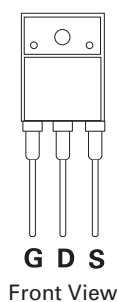


### ORDERING INFORMATION

DEVICE	MULTIPLES
ZXM64N035L3	1000

### DEVICE MARKING

- ZXM6  
4N035



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## ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DSS}$	35	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $V_{GS}=10V$ ; $T_C=25^\circ C$ )(a) ( $V_{GS}=10V$ ; $T_A=25^\circ C$ )(b)	$I_D$	13 3.5	A
Pulsed Drain Current (b)	$I_{DM}$	30	A
Continuous Source Current (Body Diode)(b)	$I_S$	2.4	A
Pulsed Source Current (Body Diode)(b)	$I_{SM}$	30	A
Power Dissipation at $T_A=25^\circ C$ (a) Linear Derating Factor	$P_D$	20 160	W mW/ $^\circ C$
Power Dissipation at $T_A=25^\circ C$ (b) Linear Derating Factor	$P_D$	1.5 12	W mW/ $^\circ C$
Operating and Storage Temperature Range	$T_j:T_{stg}$	-55 to +150	$^\circ C$

## THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Case (a)	$R_{\theta JC}$	6.25	$^\circ C/W$
Junction to Ambient (b)	$R_{\theta JA}$	83.3	$^\circ C/W$

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## ELECTRICAL CHARACTERISTICS (at $T_A = 25^\circ\text{C}$ unless otherwise stated).

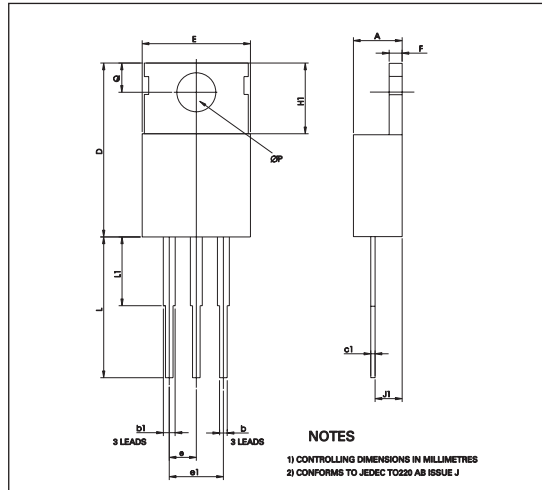
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	35			V	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$
Zero Gate Voltage Drain Current	$I_{DSS}$			1	$\mu\text{A}$	$V_{DS}=35\text{V}, V_{GS}=0\text{V}$
Gate-Body Leakage	$I_{GSS}$			100	nA	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	1.0			V	$I_D=250\mu\text{A}, V_{DS}=V_{GS}$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$			0.060 0.070	$\Omega$ $\Omega$	$V_{GS}=10\text{V}, I_D=3.7\text{A}$ $V_{GS}=4.5\text{V}, I_D=1.9\text{A}$
Forward Transconductance (1)(3)	$g_{fs}$	4.3			S	$V_{DS}=10\text{V}, I_D=1.9\text{A}$
<b>DYNAMIC (3)</b>						
Input Capacitance	$C_{iss}$		950		pF	$V_{DS}=25\text{V}, V_{GS}=0\text{V},$ $f=1\text{MHz}$
Output Capacitance	$C_{oss}$		200		pF	
Reverse Transfer Capacitance	$C_{rss}$		50		pF	
<b>SWITCHING(2) (3)</b>						
Turn-On Delay Time	$t_{d(on)}$		4.2		ns	$V_{DD}=15\text{V}, I_D=3.7\text{A}$ $R_G=6.0\Omega, V_{GS}=10\text{V}$
Rise Time	$t_r$		4.5		ns	
Turn-Off Delay Time	$t_{d(off)}$		20.5		ns	
Fall Time	$t_f$		8		ns	
Total Gate Charge	$Q_g$			27	nC	$V_{DS}=24\text{V}, V_{GS}=10\text{V},$ $I_D=3.7\text{A}$
Gate-Source Charge	$Q_{gs}$			5	nC	
Gate-Drain Charge	$Q_{gd}$			4.5	nC	
<b>SOURCE-DRAIN DIODE</b>						
Diode Forward Voltage (1)	$V_{SD}$			0.95	V	$T_J=25^\circ\text{C}, I_S=3.7\text{A},$ $V_{GS}=0\text{V}$
Reverse Recovery Time (3)	$t_{rr}$		24.5		ns	$T_J=25^\circ\text{C}, I_F=3.7\text{A},$ $di/dt=100\text{A}/\mu\text{s}$
Reverse Recovery Charge (3)	$Q_{rr}$		19.1		nC	

### NOTES

- (1) Measured under pulsed conditions. Width=300 $\mu\text{s}$ . Duty cycle  $\leq 2\%$ .
- (2) Switching characteristics are independent of operating junction temperature.
- (3) For design aid only, not subject to production testing.

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## Package Outline



## Package Dimensions

DIM	Millimetres		Inches	
	Min	Max	Min	Max
A	3.56	4.82	0.140	0.189
b	0.38	1.01	0.015	0.040
b1	1.15	1.77	0.045	0.070
c1	0.41	0.50	0.016	0.020
D	14.23	16.51	0.560	0.650
E	9.66	10.66	0.380	0.419
e	2.29	2.79	0.090	0.110
e1	4.83	5.33	0.190	0.210
F	0.51	1.39	0.20	0.055
H1	5.58	6.85	0.230	0.270
J1	2.04	2.92	0.080	0.115
L	12.70	14.73	0.500	0.580
L1	—	6.35	—	0.250
ØP	3.54	4.08	0.139	0.160
Q	2.54	3.42	0.100	0.134

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Zetex plc  
 Fields New Road  
 Chadderton  
 Oldham, OL9 8NP  
 United Kingdom  
 Telephone (44) 161 622 4422  
 Fax: (44) 161 622 4420

Zetex GmbH  
 Streifeldstraße 19  
 D-81673 München  
 Germany  
 Telefon: (49) 89 45 49 49 0  
 Fax: (49) 89 45 49 49 49

Zetex Inc  
 700 Veterans Memorial Hwy  
 Hauppauge, NY11788  
 USA  
 Telephone: (631) 360 2222  
 Fax: (631) 360 8222

Zetex (Asia) Ltd  
 3701-04 Metroplaza, Tower 1  
 Hing Fong Road  
 Kwai Fong  
 Hong Kong  
 Telephone: (852) 26100 611  
 Fax: (852) 24250 494

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