

TRIACs, 40A Snubberless and Standard

FEATURES

- High current triac
- Low thermal resistance with clip bonding
- Low thermal resistance insulation ceramic for insulated TO-3 package
- High commutation capability
- Packages are RoHS compliant

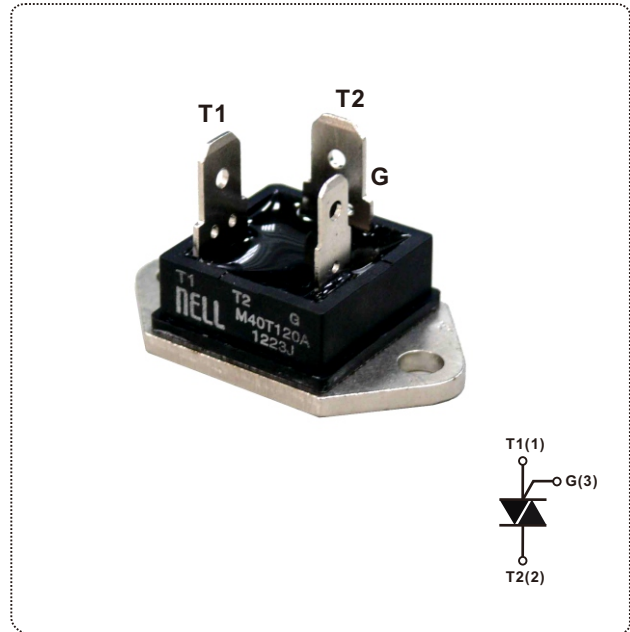
APPLICATIONS

Due to their clip assembly technique, they provide a superior performance in surge current handling capabilities.

By using an internal ceramic pad, the M40T series provides voltage insulated tab (rated at 2500VRMS) complying with UL standards.

The snubberless concept offer suppression of RC network and it is suitable for applications such as :

- Static relays
- Solid state switches
- Motor controls
- Light dimmers
- Copy machines
- Microwave ovens
- Heater controls



MAIN FEATURES

SYMBOL	VALUE	UNIT
$I_{T(RMS)}$	40	A
V_{DRM}/V_{RRM}	600 to 1200	V
$I_{GT(Q1)}$	10 to 50	mA

ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUE	UNIT
RMS on-state current (full sine wave)	$I_{T(RMS)}$		$T_c = 90^\circ\text{C}$	40	A
Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)	I_{TSM}	F = 50 Hz	t = 20 ms	400	A
		F = 60 Hz	t = 16.7 ms	420	
I^2t Value for fusing	I^2t	$t_p = 10$ ms		800	A^2s
Critical rate of rise of on-state current $I_G = 2I_{GT}$, $t_r \leq 100\text{ns}$	dI/dt	F = 100 Hz	$T_j = 125^\circ\text{C}$	50	A/ μs
Peak gate current	I_{GM}	$T_p = 20$ μs	$T_j = 125^\circ\text{C}$	4	A
Peak gate power dissipation ($t_p = 20\mu\text{s}$)	P_{GM}	$T_j = 125^\circ\text{C}$		10	W
Average gate power dissipation	$P_{G(AV)}$	$T_j = 125^\circ\text{C}$		1	
Storage temperature range	T_{stg}			- 40 to + 150	$^\circ\text{C}$
Operating junction temperature range	T_j			- 40 to + 125	

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SNUBBERLESS (3 quadrants)					
SYMBOL	TEST CONDITIONS	QUADRANT		LIMITS	UNIT
I _{GT} ⁽¹⁾	V _D = 12 V, R _L = 33Ω	I - II - III	MAX.	50	mA
V _{GT}		I - II - III		1.3	V
V _{GD}	V _D = V _{DRM} , R _L = 3.3KΩ T _j = 125°C	I - II - III	MIN.	0.2	V
I _H ⁽²⁾	I _T = 500 mA		MAX.	60	mA
I _L	I _G = 1.2 I _{GT}	I - III	MAX.	80	mA
		II		150	
dV/dt ⁽²⁾	V _D = 67% V _{DRM} , gate open, T _j = 125°C		MIN.	1000	V/μs
(dl/dt) _c ⁽²⁾	Without snubber, T _j = 125°C			20	A/ms

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STANDARD (4 quadrants)					
SYMBOL	TEST CONDITIONS	QUADRANT		LIMITS	UNIT
				B	
I _{GT} ⁽¹⁾	V _D = 12 V, R _L = 33Ω	I - II - III	MAX.	50	mA
V _{GT}		IV		100	
V _{GD}	V _D = V _{DRM} , R _L = 3.3KΩ, T _j = 125°C	ALL	MAX.	1.5	V
V _{GD}	V _D = V _{DRM} , R _L = 3.3KΩ, T _j = 125°C	ALL	MIN.	0.2	V
I _H ⁽²⁾	I _T = 500 mA		MAX.	50	mA
I _L	I _G = 1.2 I _{GT}	I - III - IV	MAX.	60	mA
		II		120	
dV/dt ⁽²⁾	V _D = 67% V _{DRM} , gate open, T _j = 125°C		MIN.	500	V/μs
(dV/dt) _c ⁽²⁾	Without snubber, T _j = 125°C		MIN.	30	V/μs

Note 1: Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: For both polarities of A2 referenced to A1.

STATIC CHARACTERISTICS					
SYMBOL	TEST CONDITIONS			VALUE	UNIT
V _{TM} ⁽²⁾	I _{TM} = 60 A, t _p = 380 μs	T _j = 25°C	MAX.	1.55	V
V _{I0} ⁽²⁾	Threshold voltage	T _j = 125°C	MAX.	0.85	V
R _d ⁽²⁾	Dynamic resistance	T _j = 125°C	MAX.	10	mΩ
I _{DRM} I _{RDM}	V _D = V _{DRM} V _R = V _{RDM}	T _j = 25°C	MAX.	10	μA
		T _j = 125°C		5	mA

THERMAL RESISTANCE			
SYMBOL		VALUE	UNIT
$R_{th(j-c)}$	Junction to case (AC)	0.8	°C/W
$R_{th(j-a)}$	Junction to ambient	50	

S = Copper surface under tab.

PRODUCT SELECTOR							
PART NUMBER	VOLTAGE (xx)				SENSITIVITY	TYPE	PACKAGE
	600 V	800 V	1000 V	1200 V			
M40TxxA	V	V	V	V	50 mA	Snubberless	TO-3
M40TxxA-B	V	V	V	V	50 mA	Standard	TO-3

ORDERING INFORMATION					
ORDERING TYPE	MARKING	PACKAGE	WEIGHT	BASE Q'TY	DELIVERY MODE
M40TxxA	M40TxxA	TO-3	23g	50	BOX
M40TxxA-B	M40TxxA-B	TO-3	23g	50	BOX

Note : xx = voltage

ORDERING INFORMATION SCHEME	
<p>M 40 T 60 A - B</p>	<p>Module type M = TO-3 Fast-on package</p> <p>Current 40 = 40A</p> <p>Triac series</p> <p>Voltage 60 = 600V 80 = 800V 100 = 1000V 120 = 1200V</p> <p>Assembly type A = Soldering Assembly</p> <p>I_{GT} Sensitivity B = 50mA Standard (4Q) Blank = 50mA Snubberless (3Q)</p>

Fig.1 Maximum power dissipation versus on-state RMS current (full cycle)

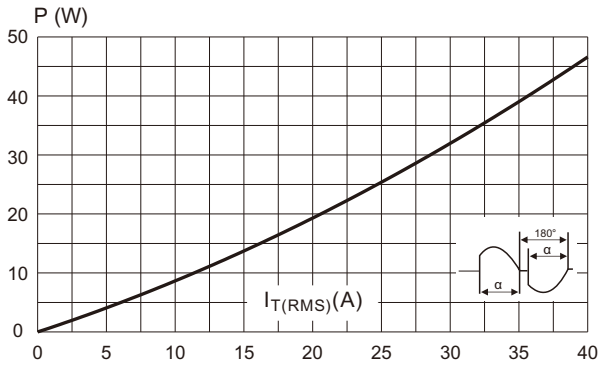


Fig.2 On-state RMS current versus case temperature (full cycle)

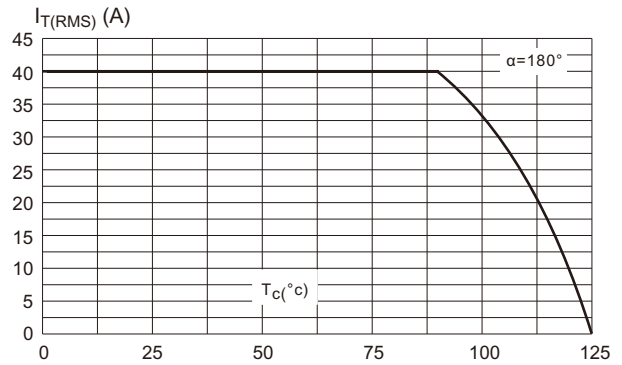


Fig.3 Relative variation of thermal impedance versus pulse duration.

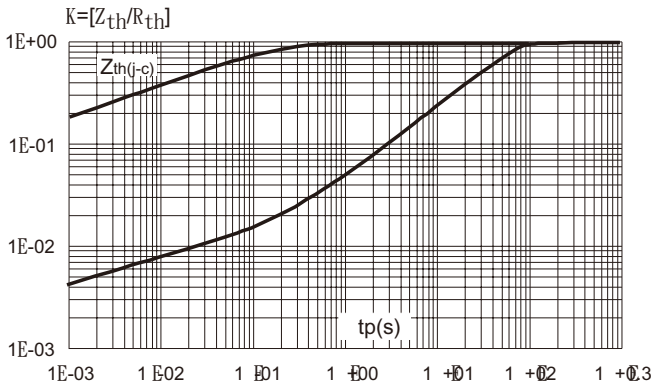


Fig.4 On-state characteristics (maximum values).

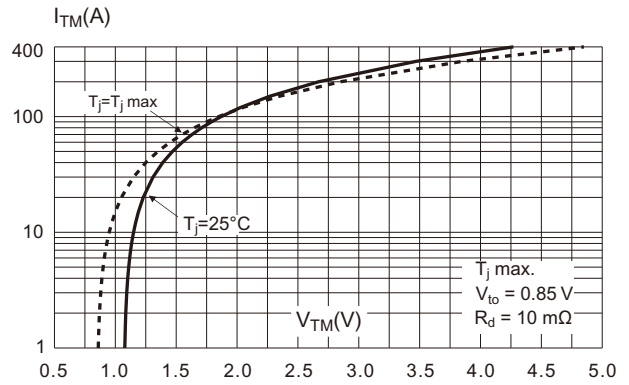


Fig.5 Surge peak on-state current versus number of cycles.

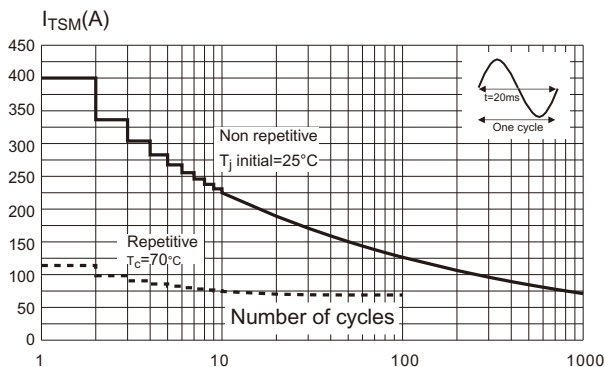


Fig.6 Non-repetitive surge peak on-state current for a sinusoidal pulse and corresponding value of I^2t.

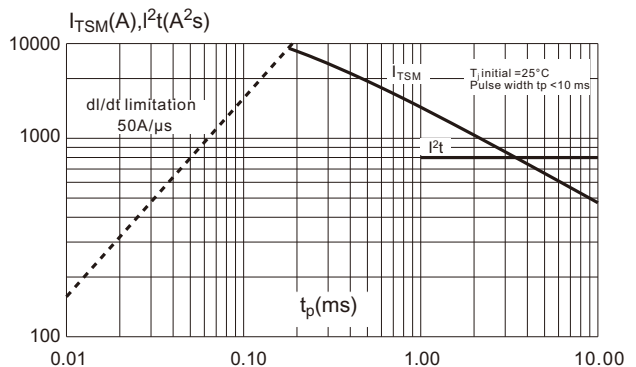


Fig.7 Relative variation of gate trigger, holding and latching current versus junction temperature.

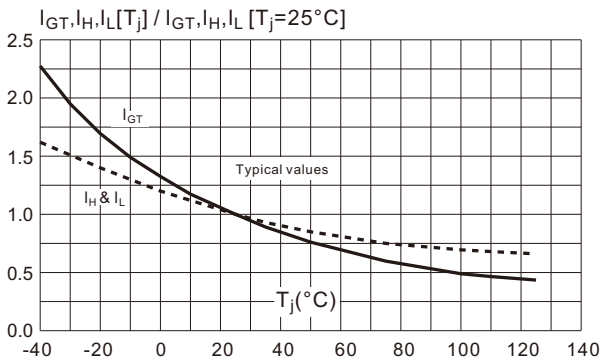


Fig.8 Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values).

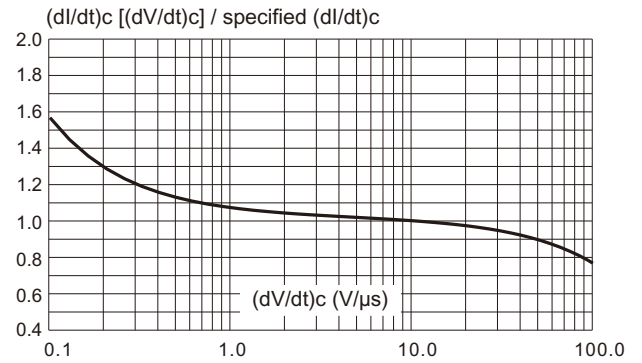
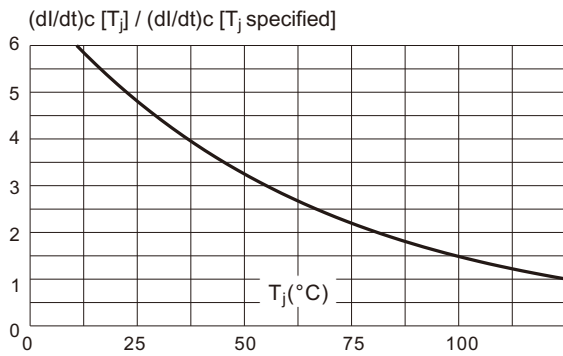


Fig.9 Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$.



Case Style

