

# NCP4629

## 500 mA, Wide Input Range, LDO Linear Voltage Regulator

The NCP4629 is a CMOS 500 mA LDO linear voltage regulator which features a high input voltage range while maintaining a low quiescent current. Several protection features like current limiting and thermal shutdown are fully integrated to create a versatile and robust device. A high maximum input voltage (36 V) and wide temperature range (-40°C to 105°C) makes the NCP4629 an ideal choice for high power industrial applications.

### Features

- Operating Input Voltage Range: 4 V to 24 V
- Output Voltage Range: 3.0 to 12.0 V (available in 0.1 V steps)
- $\pm 2\%$  Output Voltage Accuracy
- Output Current: min. 500 mA ( $V_{IN} = V_{OUT} + 1$  V)
- Line Regulation: 0.05%/V
- Current Limit Circuit
- Thermal Shutdown Circuit
- Available in SOT-89-5 and DPAK5 Package
- These are Pb-Free Devices

### Typical Applications

- Home appliances, industrial equipment
- Cable boxes, satellite receivers, entertainment systems
- Car audio equipment, navigation systems
- Notebook adaptors, LCD TVs, cordless phones and private LAN systems
- Office equipment: copiers, printers, facsimiles, scanners, projectors, monitors

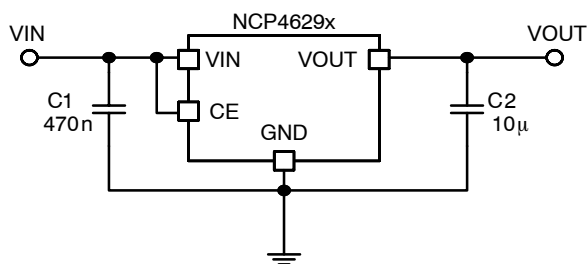


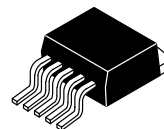
Figure 1. Typical Application Schematic



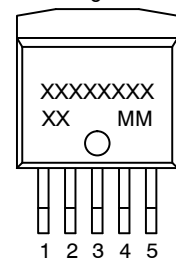
ON Semiconductor™

<http://onsemi.com>

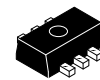
### MARKING DIAGRAMS



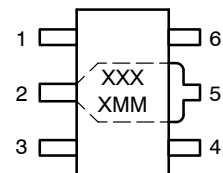
DPACK-5  
CASE 369AE



Heatsink surface shown as terminal 6  
is internally connected to Pin 3



SOT-89 5  
CASE 528AB



Heatsink surface shown as terminal 6  
is internally connected to Pin 2

XXXXX = Specific Device Code  
MM = Date Code

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

# NCP4629

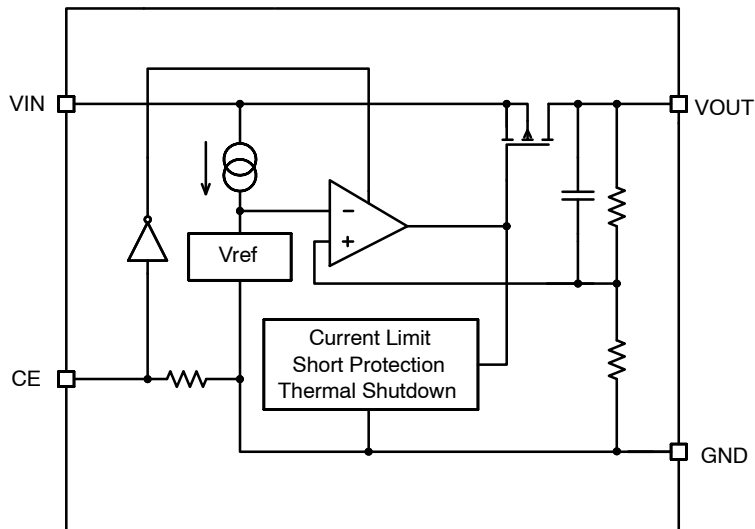


Figure 2. Simplified Schematic Block Diagram

## PIN FUNCTION DESCRIPTION

Pin No. SOT-89	Pin No. DPAK	Pin Name	Description
1	1	VIN	Input pin
2	2	GND*	Ground pin, all ground pins must be connected together when it is mounted on board
3	3	GND*	Ground pin, all ground pins must be connected together when it is mounted on board
4	4	CE	Chip enable pin ("H" active)
5	5	VOUT	Output pin
6		GND	Heatsink surface is internally connected to Pin 2 – GND
	6	GND	Heatsink surface is internally connected to Pin 3 – GND

\*Pin no.2 – GND and pin no.3 – GND of SOT-89 and DPAK-5 packages must be wired to the GND line when it is mounted on board.

## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	$V_{IN}$	-0.3 to 36	V
Output Voltage	$V_{OUT}$	-0.3 to $V_{IN} \leq 36$	V
Chip Enable Input	$V_{CE}$	-0.3 to $V_{IN} \leq 36$	V
Power Dissipation SOT-89-5	$P_D$	900	mW
Power Dissipation DPAK-5		1900	
Junction Temperature	$T_J$	-40 to 150	°C
Storage Temperature	$T_{STG}$	-55 to 125	°C
ESD Capability, Human Body Model (Note 2)	$ESD_{HBM}$	2000	V
ESD Capability, Machine Model (Note 2)	$ESD_{MM}$	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Duration time = 200 ms
2. This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)  
 ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)  
 Latch-up Current Maximum Rating tested per JEDEC standard: JESD78.

# NCP4629

## THEMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOT-89 Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	111	$^{\circ}\text{C}/\text{W}$
Thermal Characteristics, DPAK Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	53	$^{\circ}\text{C}/\text{W}$

## ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit		
Operating Input Voltage		$V_{IN}$	4		24	V		
Output Voltage	$V_{IN} = V_{OUT} + 1\text{ V}$ , $I_{OUT} = 100\text{ mA}$	$V_{OUT}$	x0.98		x1.02	V		
Output Voltage Temp. Coefficient	$V_{IN} = V_{OUT} + 2\text{ V}$ , $I_{OUT} = 100\text{ }\mu\text{A}$ , $T_A = -40$ to $105^{\circ}\text{C}$			$\pm 100$		ppm/ $^{\circ}\text{C}$		
Line Regulation	$V_{IN} = V_{OUT} + 1\text{ V}$ to $24\text{ V}$ , $I_{OUT} = 10\text{ mA}$	$\text{LineReg}$		0.05	0.10	%/V		
Load Regulation	$V_{IN} = V_{OUT} + 2\text{ V}$ , $I_{OUT} = 0.1\text{ mA}$ to $200\text{ mA}$	$\text{LoadReg}$		25	60	mV		
Dropout Voltage	$I_{OUT} = 200\text{ mA}$	$V_{DO}$			0.135	0.225	V	
				$3.0\text{ V} \leq V_{OUT} < 5.0\text{ V}$		0.115		0.180
				$5.0\text{ V} \leq V_{OUT} < 9.0\text{ V}$		0.095		0.155
	$8.0\text{ V} \leq V_{OUT} \leq 12.0\text{ V}$							
Output Current	$V_{IN} = V_{OUT} + 1\text{ V}$	$I_{OUT}$	500			mA		
Short Current Limit	$V_{OUT} = 0\text{ V}$	$I_{SC}$		65		mA		
Quiescent Current	$V_{IN} = V_{OUT} + 1\text{ V}$ , $V_{IN} = V_{CE}$	$I_Q$		70	130	$\mu\text{A}$		
Standby Current	$V_{IN} = 24\text{ V}$ , $V_{CE} = 0\text{ V}$	$I_{STB}$		0.1	1	$\mu\text{A}$		
CE Pin Threshold Voltage	CE Input Voltage "H"	$V_{CEH}$	2.0		$V_{IN}$	V		
	CE Input Voltage "L"	$V_{CEL}$	0		0.4			
Thermal Shutdown Temperature		$T_{SD}$		160		$^{\circ}\text{C}$		
Thermal Shutdown Release Temperature		$T_{SR}$		135		$^{\circ}\text{C}$		
Power Supply Rejection Ratio	$V_{IN} = V_{OUT} + 2.0\text{ V}$ , $\Delta V_{IN\_PK-PK} = 0.5\text{ V}$ , $I_{OUT} = 100\text{ mA}$ , $f = 1\text{ kHz}$	$\text{PSRR}$			60	dB		
				$V_{OUT} \leq 6.0\text{ V}$			50	
Output Noise Voltage	$V_{OUT} = 5.0\text{ V}$ , $I_{OUT} = 30\text{ mA}$ , $f = 10\text{ Hz}$ to $100\text{ kHz}$	$V_{NOISE}$		125		$\mu\text{V}_{rms}$		

TYPICAL CHARACTERISTICS

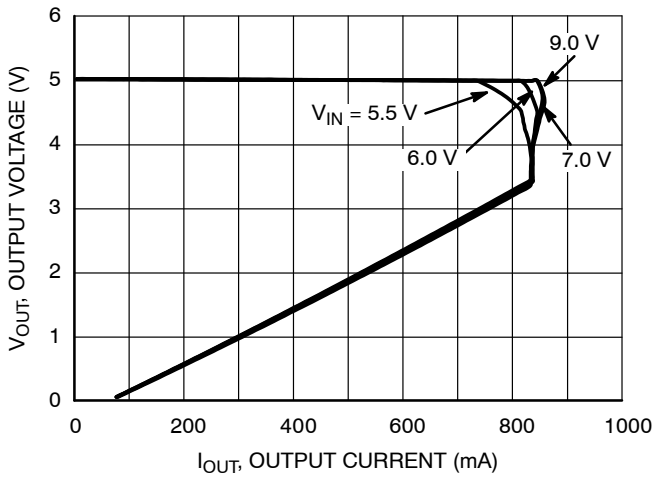


Figure 3. Output Voltage vs. Output Current,  $V_{OUT} = 5\text{ V}$

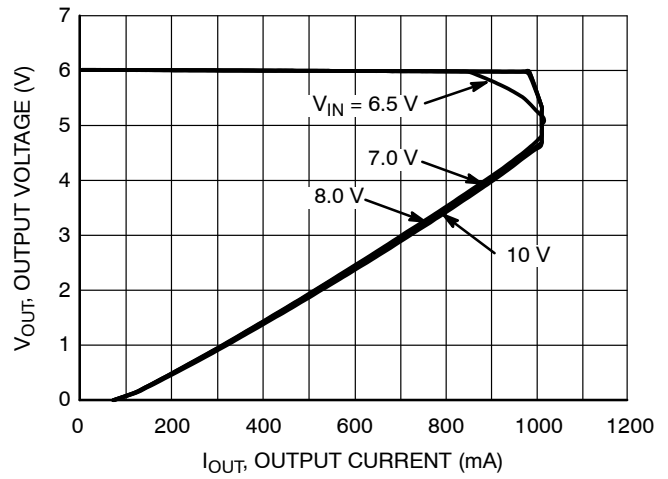


Figure 4. Output Voltage vs. Output Current,  $V_{OUT} = 6\text{ V}$

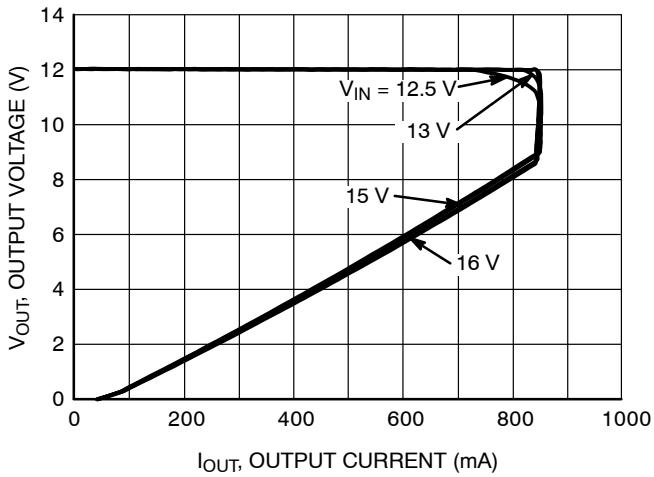


Figure 5. Output Voltage vs. Output Current,  $V_{OUT} = 12\text{ V}$

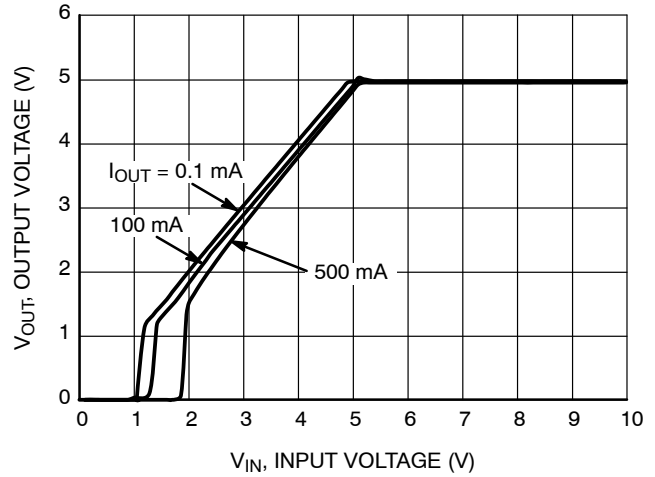


Figure 6. Output Voltage vs. Input Voltage,  $V_{OUT} = 5\text{ V}$

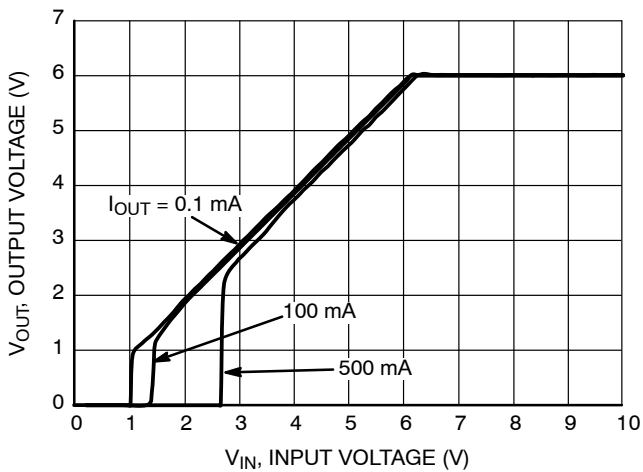


Figure 7. Output Voltage vs. Input Voltage,  $V_{OUT} = 6\text{ V}$

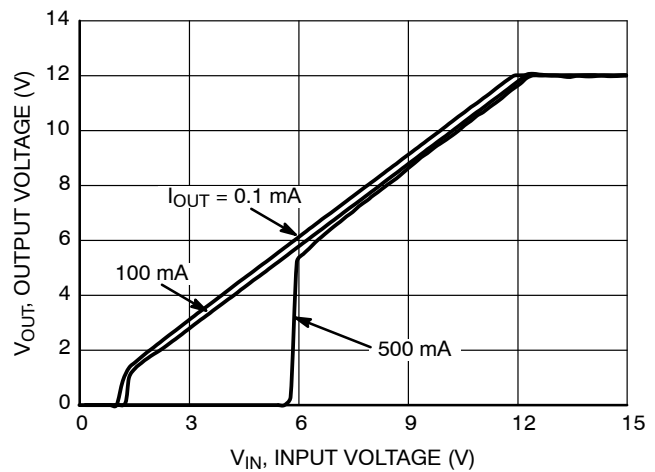


Figure 8. Output Voltage vs. Input Voltage,  $V_{OUT} = 12\text{ V}$

TYPICAL CHARACTERISTICS

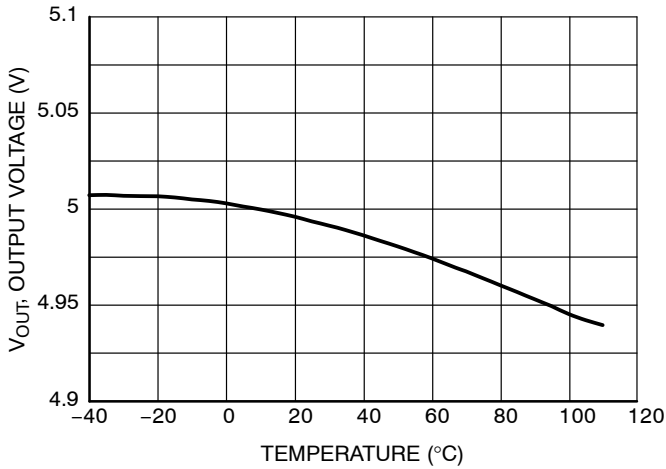


Figure 9. Output Voltage vs. Temperature,  $V_{OUT} = 5\text{ V}$

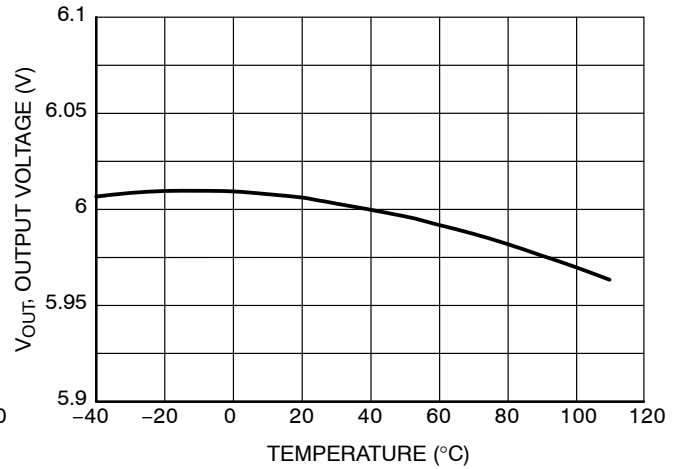


Figure 10. Output Voltage vs. Temperature,  $V_{OUT} = 6\text{ V}$

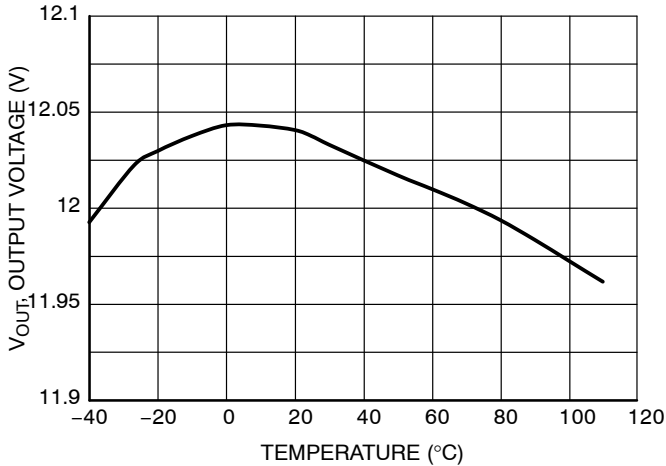


Figure 11. Output Voltage vs. Temperature,  $V_{OUT} = 12\text{ V}$

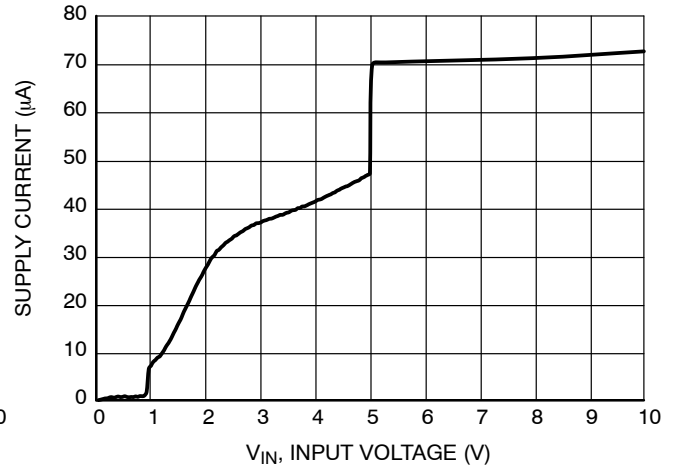


Figure 12. Supply Current vs. Input Voltage,  $V_{OUT} = 5\text{ V}$

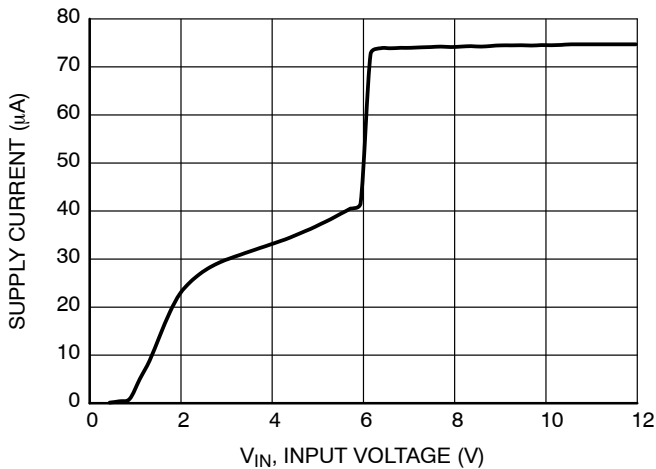


Figure 13. Supply Current vs. Input Voltage,  $V_{OUT} = 6\text{ V}$

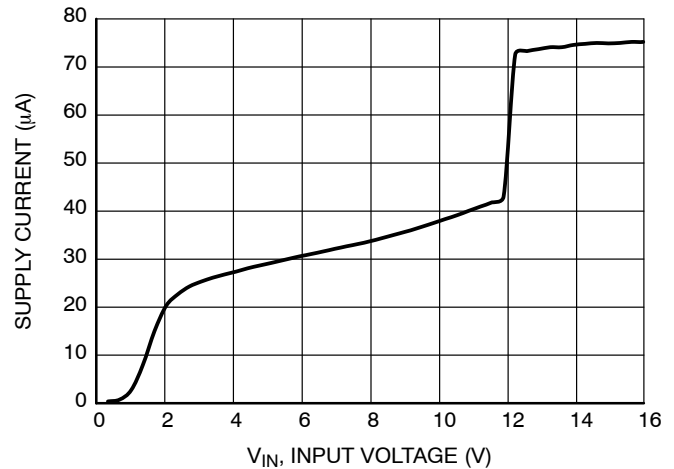


Figure 14. Supply Current vs. Input Voltage,  $V_{OUT} = 12\text{ V}$

TYPICAL CHARACTERISTICS

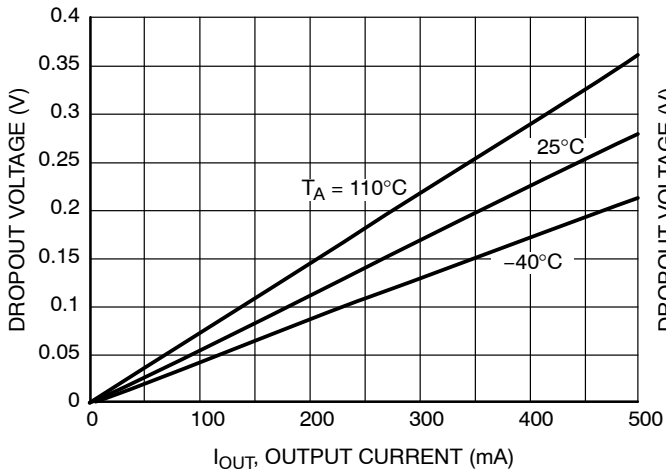


Figure 15. Dropout Voltage vs. Input Current,  $V_{OUT} = 5\text{ V}$

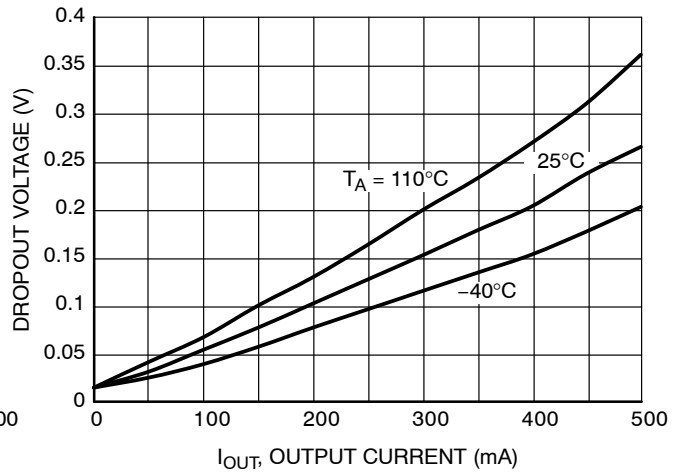


Figure 16. Dropout Voltage vs. Input Current,  $V_{OUT} = 6\text{ V}$

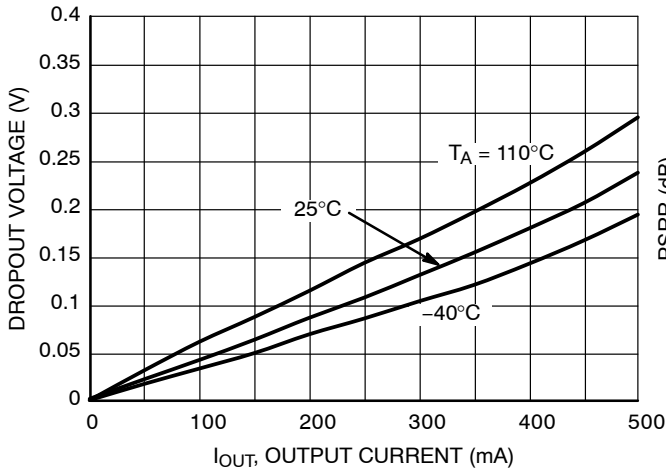


Figure 17. Dropout Voltage vs. Input Current,  $V_{OUT} = 12\text{ V}$

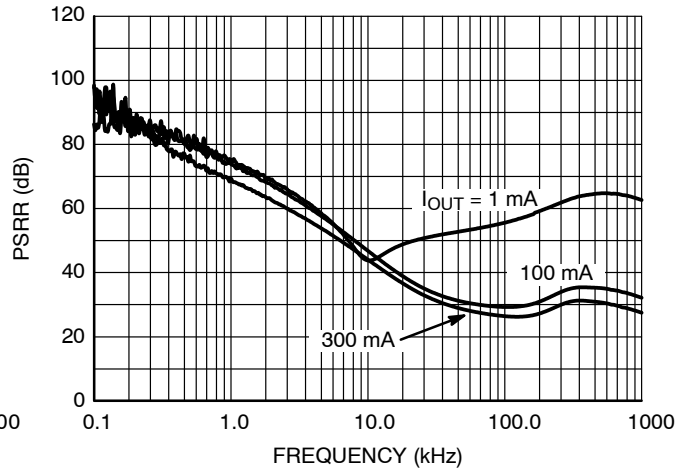


Figure 18. Ripple Rejection vs. Frequency,  $V_{OUT} = 5\text{ V}$

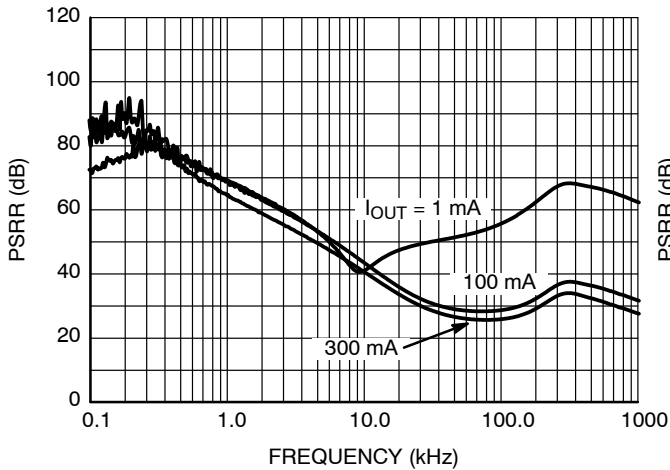


Figure 19. Ripple Rejection vs. Frequency,  $V_{OUT} = 6\text{ V}$

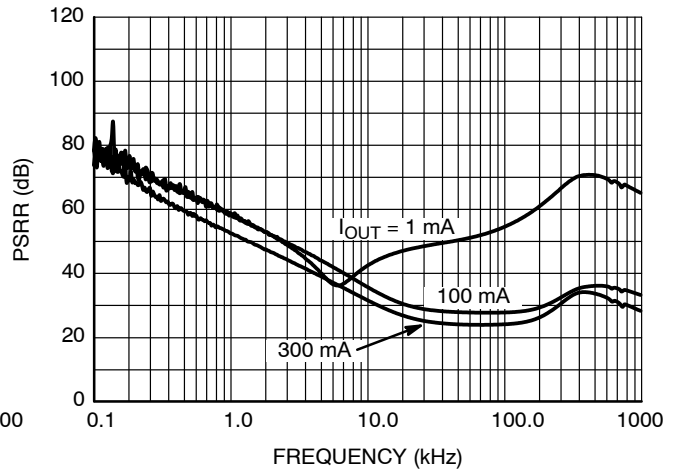


Figure 20. Ripple Rejection vs. Frequency,  $V_{OUT} = 12\text{ V}$

TYPICAL CHARACTERISTICS

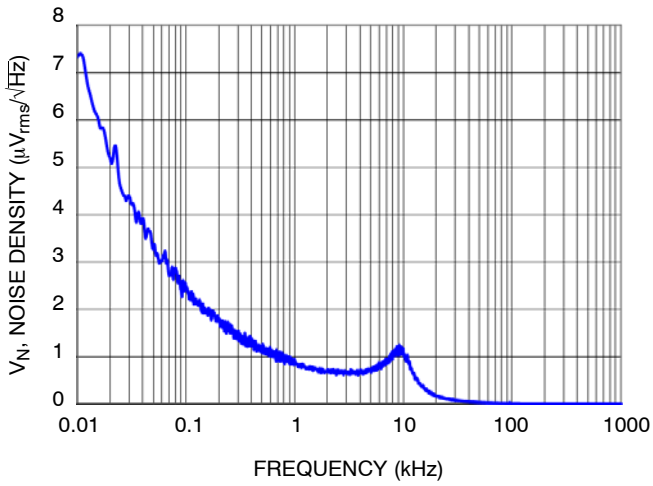


Figure 21. Output Noise Density,  $V_{OUT} = 5\text{ V}$ ,  
 $V_{IN} = 6.0\text{ V}$ ,  $I_{OUT} = 30\text{ mA}$

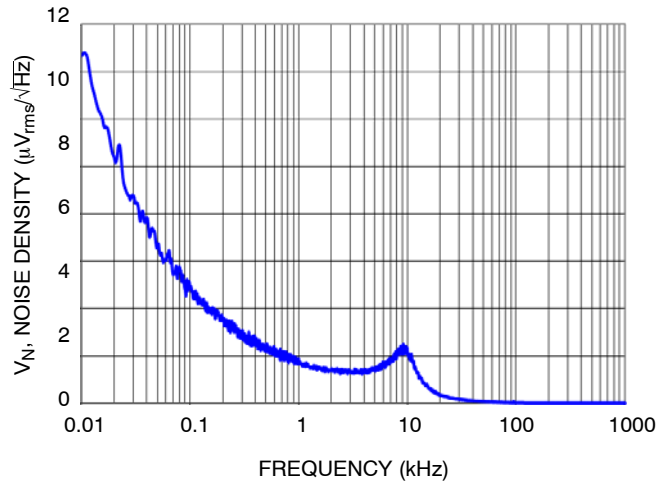


Figure 22. Output Noise Density,  $V_{OUT} = 6\text{ V}$ ,  
 $V_{IN} = 7.0\text{ V}$ ,  $I_{OUT} = 30\text{ mA}$

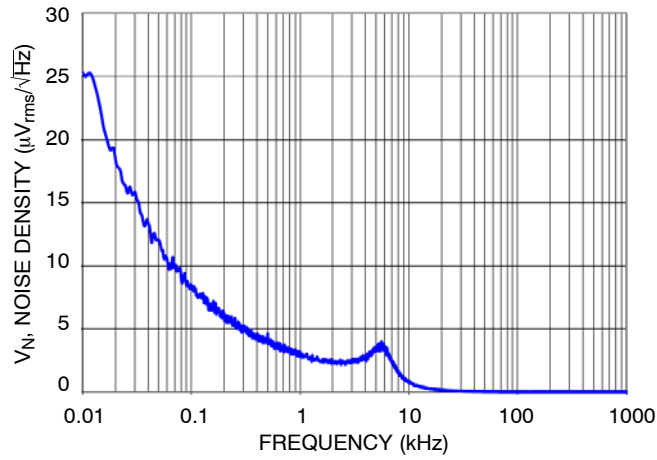


Figure 23. Output Noise Density,  $V_{OUT} = 12\text{ V}$ ,  
 $V_{IN} = 13\text{ V}$ ,  $I_{OUT} = 30\text{ mA}$

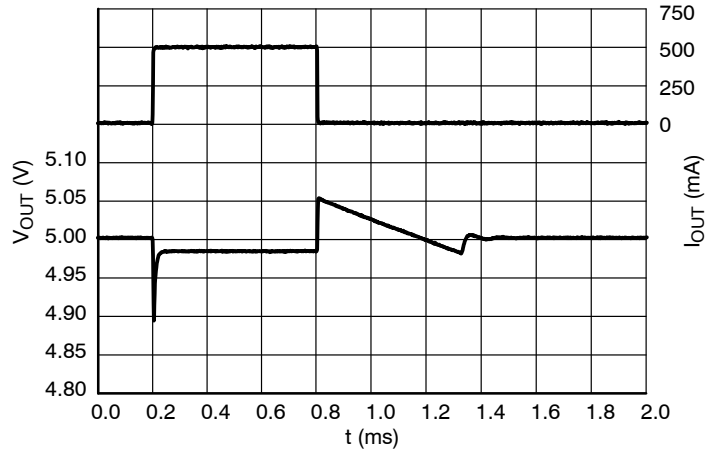
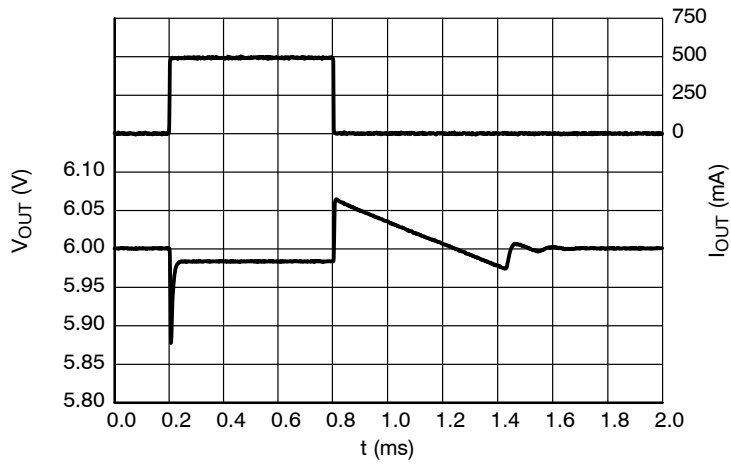


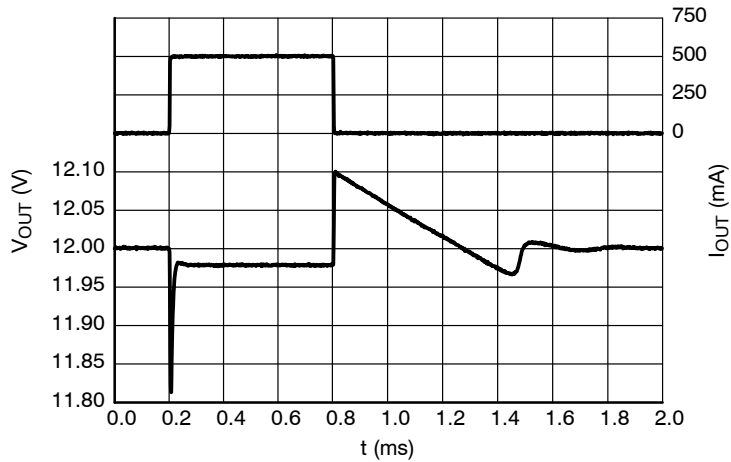
Figure 24. Load Transient Response at Output  
Current Step 1 mA to 500 mA,  $V_{OUT} = 5\text{ V}$

# NCP4629

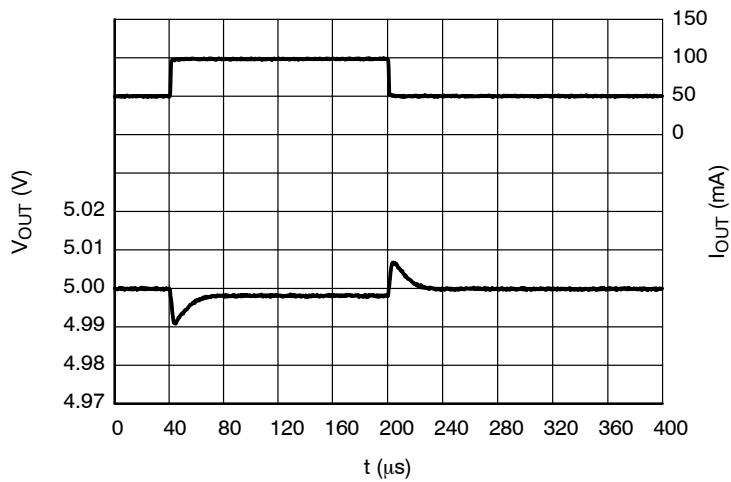
## TYPICAL CHARACTERISTICS



**Figure 25. Load Transient Response at Output Current Step 1 mA to 500 mA, V<sub>OUT</sub> = 6 V**



**Figure 26. Load Transient Response at Output Current Step 1 mA to 500 mA, V<sub>OUT</sub> = 12 V**

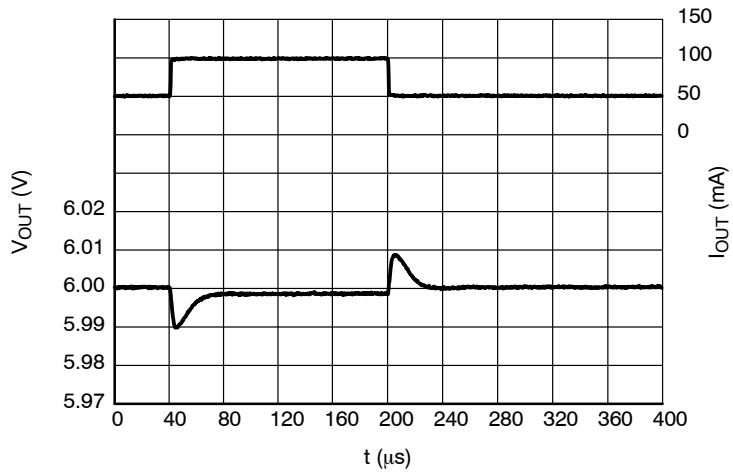


**Figure 27. Load Transient Response at Output Current Step 50 mA to 100 mA, V<sub>OUT</sub> = 5 V**

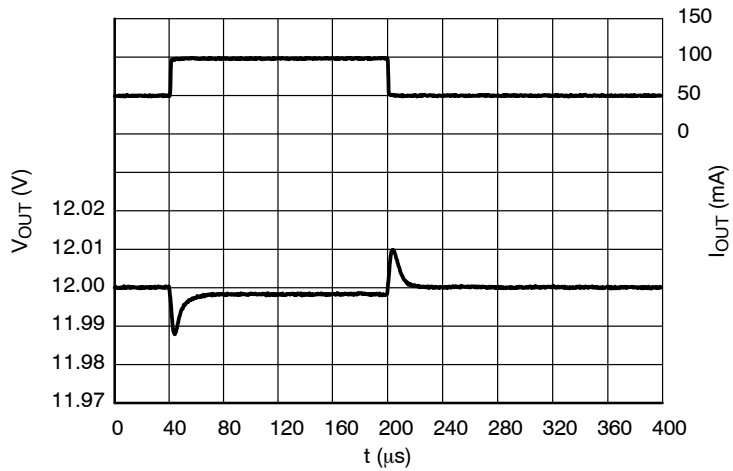


# NCP4629

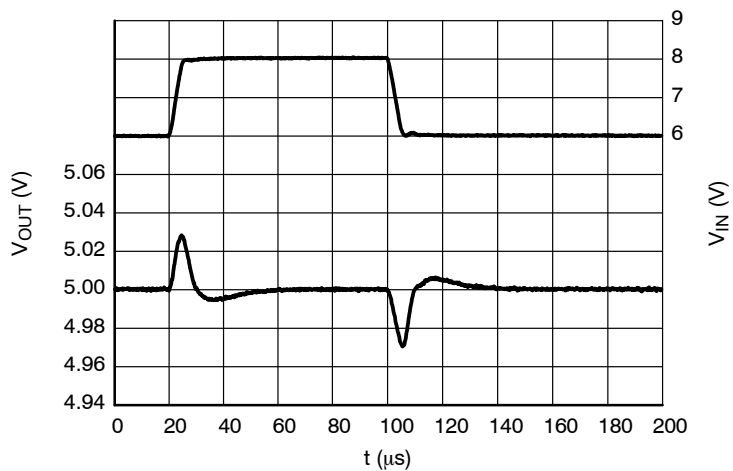
## TYPICAL CHARACTERISTICS



**Figure 28. Load Transient Response at Output Current Step 50 mA to 100 mA,  $V_{\text{OUT}} = 6 \text{ V}$**



**Figure 29. Load Transient Response at Output Current Step 50 mA to 100 mA,  $V_{\text{OUT}} = 12 \text{ V}$**



**Figure 30. Line Transient Response,  $V_{\text{OUT}} = 5 \text{ V}$**

# NCP4629

## TYPICAL CHARACTERISTICS

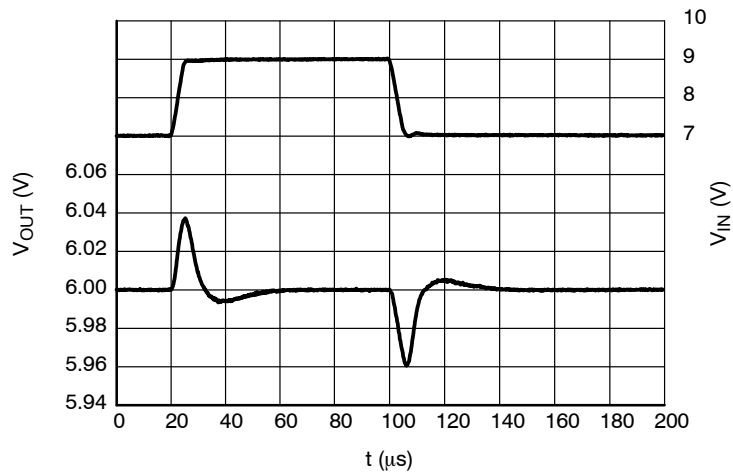


Figure 31. Line Transient Response,  $V_{OUT} = 6\text{ V}$

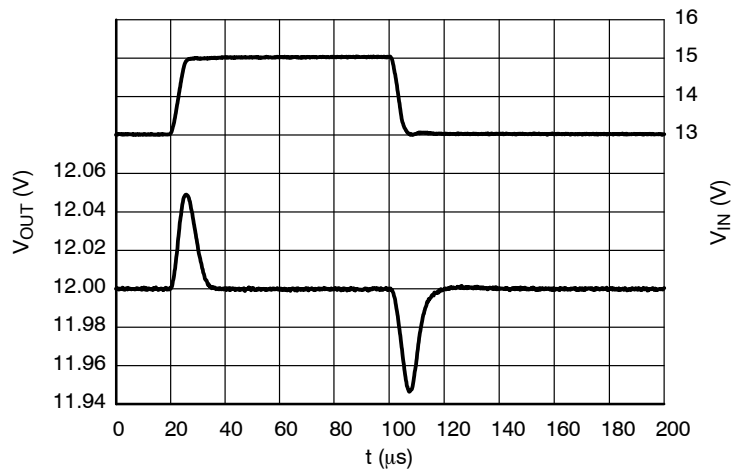


Figure 32. Line Transient Response,  
 $V_{OUT} = 12\text{ V}$

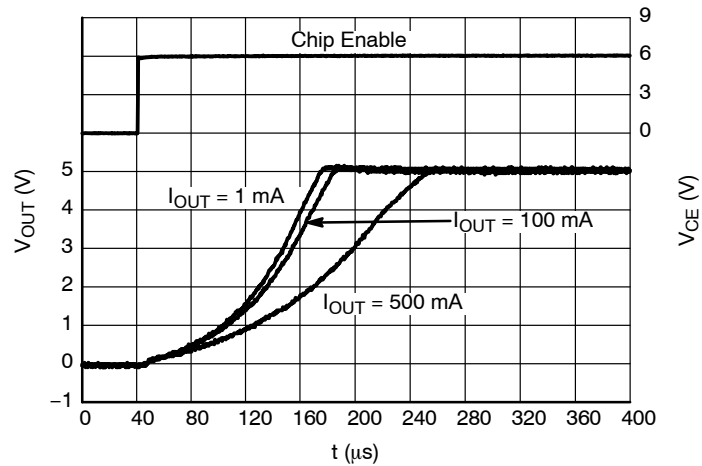


Figure 33. Turn-on Behavior with CE,  
 $V_{OUT} = 5\text{ V}$

# NCP4629

## TYPICAL CHARACTERISTICS

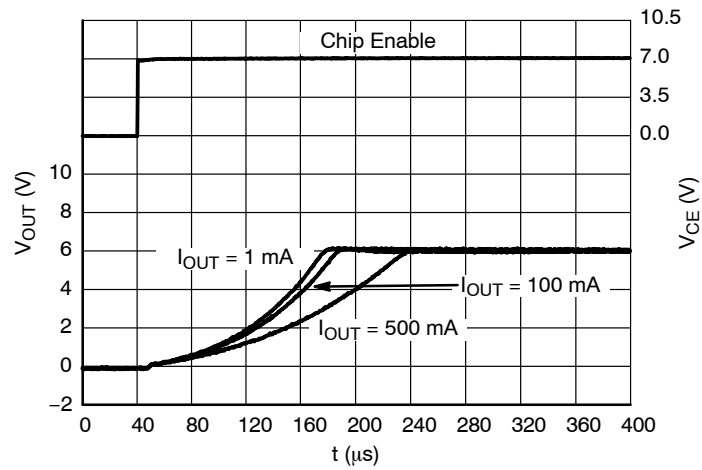


Figure 34. Turn-on Behavior with CE,  
 $V_{OUT} = 6\text{ V}$

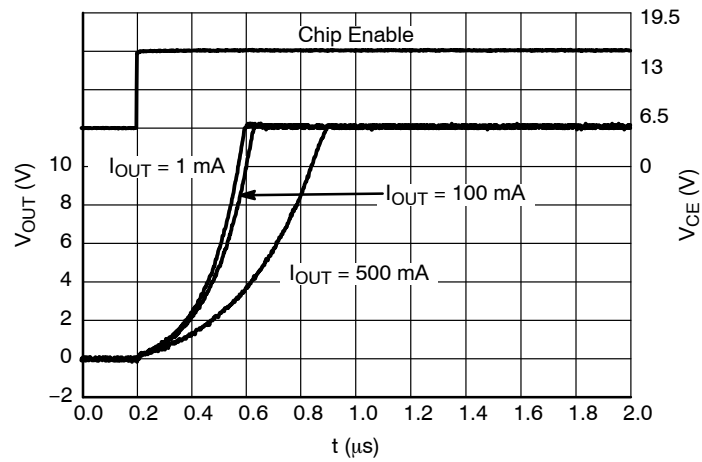


Figure 35. Turn-on Behavior with CE,  
 $V_{OUT} = 12\text{ V}$

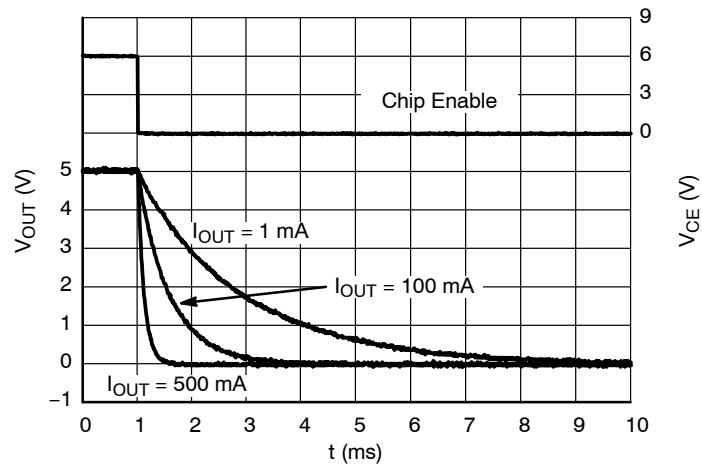


Figure 36. Turn-off Behavior with CE,  
 $V_{OUT} = 5\text{ V}$

TYPICAL CHARACTERISTICS

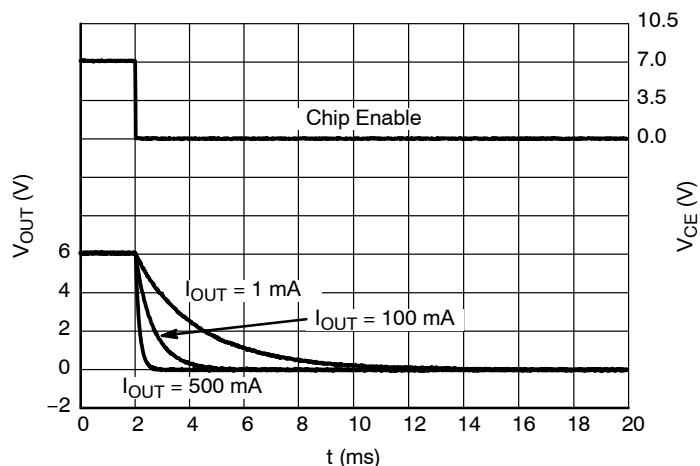


Figure 37. Turn-off Behavior with CE,  $V_{OUT} = 6\text{ V}$

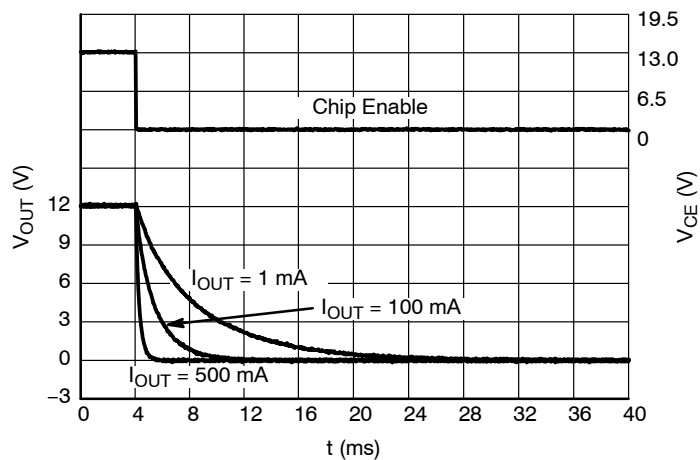


Figure 38. Turn-off Behavior with CE,  $V_{OUT} = 12\text{ V}$

APPLICATION INFORMATION

A typical application circuit for NCP4629 series is shown in Figure 39.

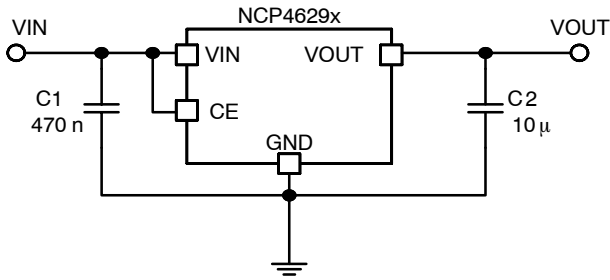


Figure 39. Typical Application Schematic

When VOUT voltage could be higher than VIN voltage it is necessary to use protective diode D1. If there is possibility that VOUT voltage could be negative then it is necessary to use schottky diode D2. See Figure 40 for details. Do not force the voltage to the VOUT pin.

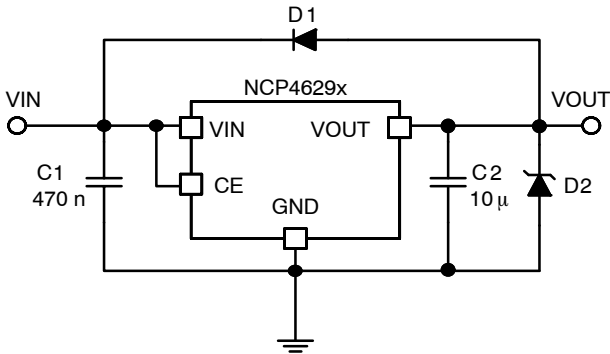


Figure 40. Typical Application Schematic with Protective Diodes

Input Decoupling Capacitor (C1)

A 470 nF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4629. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

A 10 μF ceramic output decoupling capacitor is sufficient to achieve stable operation of the IC. If tantalum capacitor is used, and its ESR is high, the loop oscillation may result. The capacitor should be connected as close as possible to the output and ground pin. Larger values and lower ESR improves dynamic parameters.

Enable Operation

The enable pin CE may be used for turning the regulator on and off. The IC is switched on when a high level voltage is applied to the CE pin. The enable pin has an internal pull down current source. If the enable function is not needed connect CE pin to VIN.

Thermal

As a power across the IC increase, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature increase for the part. When the device has good thermal conductivity through the PCB the junction temperature will be relatively low in high power dissipation applications.

The IC includes internal thermal shutdown circuit that stops operation of regulator, if junction temperature is higher than 160°C. After that, when junction temperature decreases below 135°C, the operation of voltage regulator would restart. While high power dissipation condition is, the regulator starts and stops repeatedly and protects itself against overheating.

PCB layout

Pins number 2 and 3 must be wired to the GND plane while it is mounted on board. Make VIN and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1 and C2 as close as possible to the IC, and make wiring as short as possible.

ORDERING INFORMATION

Device	Nominal Output Voltage	Description	Marking	Package	Shipping†
NCP4629HDT050T5G	5.0 V	Enable High	C1J050B	DPAK-5 (Pb-Free)	3000 / Tape & Reel
NCP4629HDT060T5G	6.0 V	Enable High	C1J060B	DPAK-5 (Pb-Free)	3000 / Tape & Reel
NCP4629HDT120T5G	12.0 V	Enable High	C1J120B	DPAK-5 (Pb-Free)	3000 / Tape & Reel

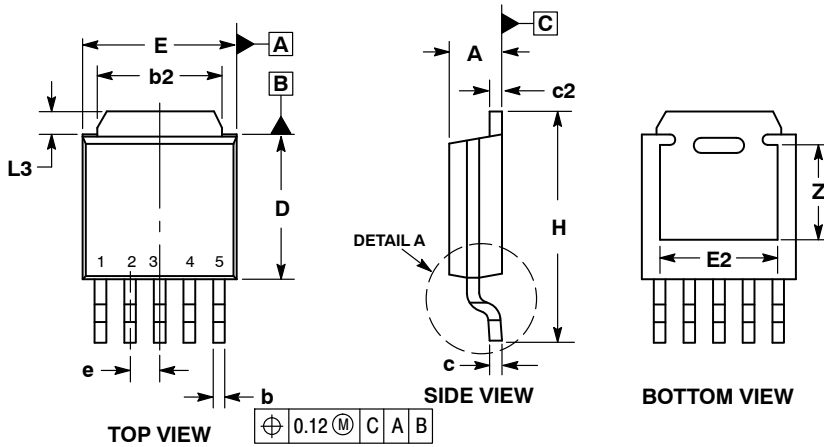
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*To order other package and voltage variants, please contact your ON Semiconductor sales representative.

# NCP4629

## PACKAGE DIMENSIONS

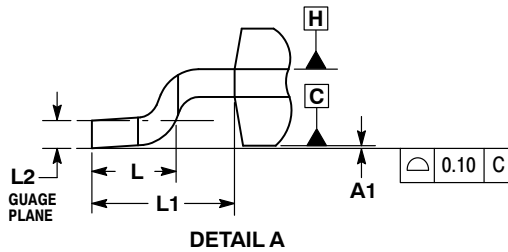
DPAK-5 (TO-252, 5 LEAD)  
CASE 369AE  
ISSUE O



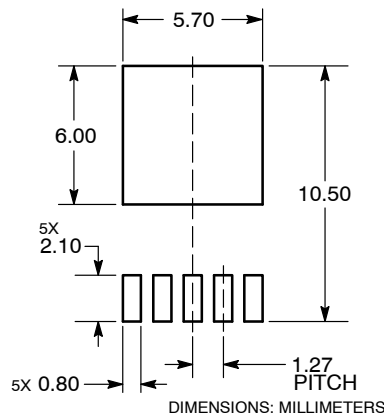
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL, WITHIN DIMENSIONS b3, E2, L3 AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. THESE DIMENSIONS TO BE MEASURED AT DATUM H.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

MILLIMETERS		
DIM	MIN	MAX
A	2.10	2.50
A1	0.00	0.13
b	0.40	0.60
b2	5.14	5.54
c	0.40	0.60
c2	0.40	0.60
D	5.90	6.30
E	6.40	6.80
E2	5.04	REF
e	1.27	BSC
H	9.60	10.20
L	1.39	1.78
L1	2.50	2.90
L2	0.51	BSC
L3	0.90	1.30
Z	2.74	REF



**RECOMMENDED SOLDERING FOOTPRINT\***

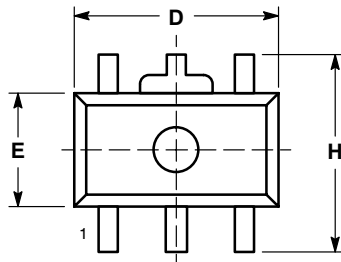


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

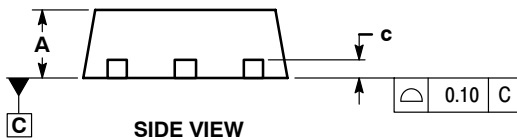
# NCP4629

## PACKAGE DIMENSIONS

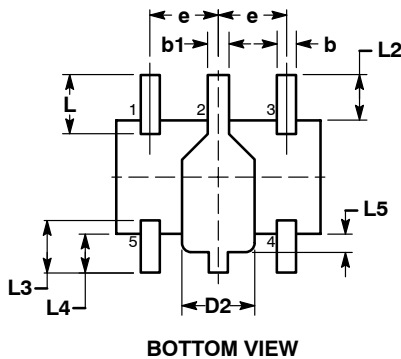
### SOT-89, 5 LEAD CASE 528AB ISSUE O



TOP VIEW



SIDE VIEW



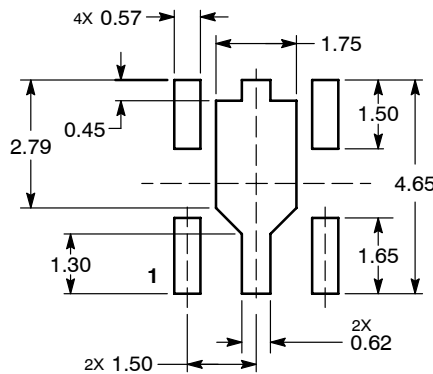
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS INCLUDES LEAD FINISH.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. DIMENSIONS L, L2, L3, L4, L5, AND H ARE MEASURED AT DATUM PLANE C.

MILLIMETERS		
DIM	MIN	MAX
A	1.40	1.60
b	0.32	0.52
b1	0.37	0.57
c	0.30	0.50
D	4.40	4.60
D2	1.40	1.80
E	2.40	2.60
e	1.40	1.60
H	4.25	4.45
L	1.10	1.50
L2	0.80	1.20
L3	0.95	1.35
L4	0.65	1.05
L5	0.20	0.60

### RECOMMENDED MOUNTING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative