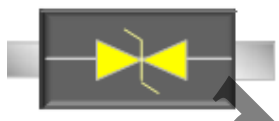
Bi-directional ESD Protection Diode

FEATURES

- Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- Meet IEC61000-4-4 (EFT) rating. 40A (5/50ns)
- Protects one Bi-directional I/O line
- Working Voltage : 5V
- Pb free version and RoHS compliant
- Packing code with suffix "G" means green compound (halogen-free)

SOD-523F



MECHANICAL DATA

- Case: SOD-523F small outline plastic package
- Terminal: Matte tin plated, lead free., solderable per MIL-STD-202, Method 208 guaranteed
- High temperature soldering guaranteed : 260°C/10s
- Weight: 2 ± 0.5 mg
- Marking code: TB

APPLICATIONS

- Cell Phone Handsets and Accessories
- Notebooks, Desktops, and Servers
- Personal Digital Assistants (PDA's)
- Portable Instrumentation
- Microprocessor Based Equipment

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	VALUE	UNIT
Peak Pulse Power (tp=8/20μs waveform)	P_{PP}	100	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	± 15 ± 8	KV
Junction and Storage Temperature Range	T_J , T_{STG}	-55 to +150	°C

PARAMETER		SYMBOL	MIN	MAX	UNIT
Reverse Stand-Off Voltage		V_{RWM}	-	5	V
Reverse Breakdown Voltage	I_R = 1 mA	$V_{(BR)}$	6	-	V
Reverse Leakage Current	V_R = 5 V	I_R	-	1	μA
Clamping Voltage	I_{PP} = 1 A	V_C	-	10	V
	I_{PP} = 5 A		-	15	
Junction Capacitance	V_R = 0 V , f = 1.0 MHz	C_J	35		pF

RATINGS AND CHARACTERISTICS CURVES

(T_A=25°C unless otherwise noted)

Fig. 1 Non-Repetitive Peak Pulse Power VS. Pulse Time

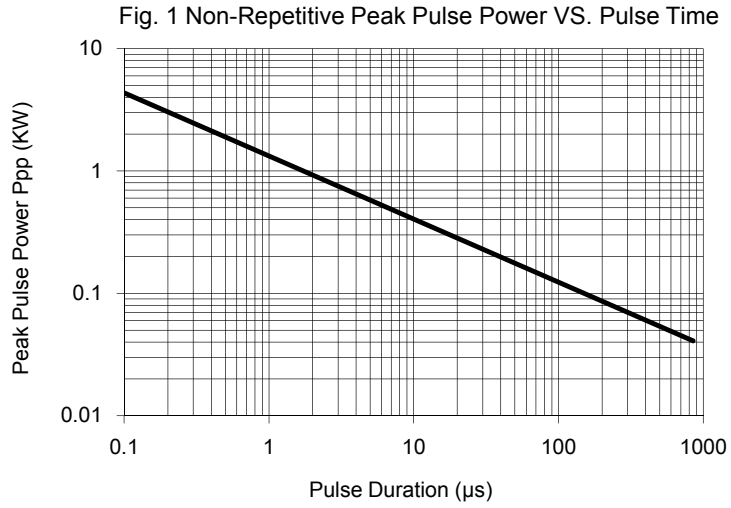


Fig. 2 Pulse Waveform

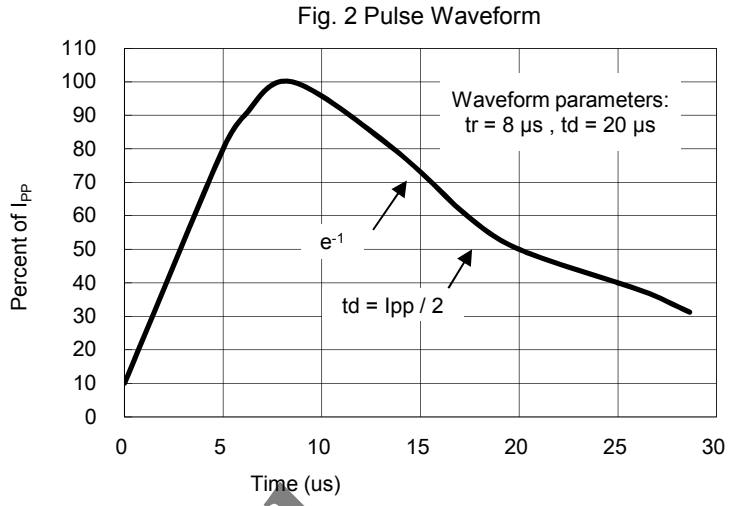


Fig. 3 Admissible Power Dissipation Curve

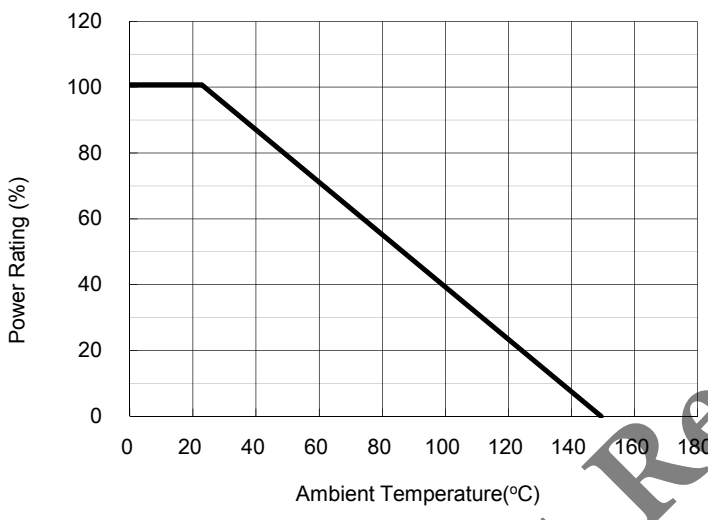


Fig. 4 Typical Junction Capacitance

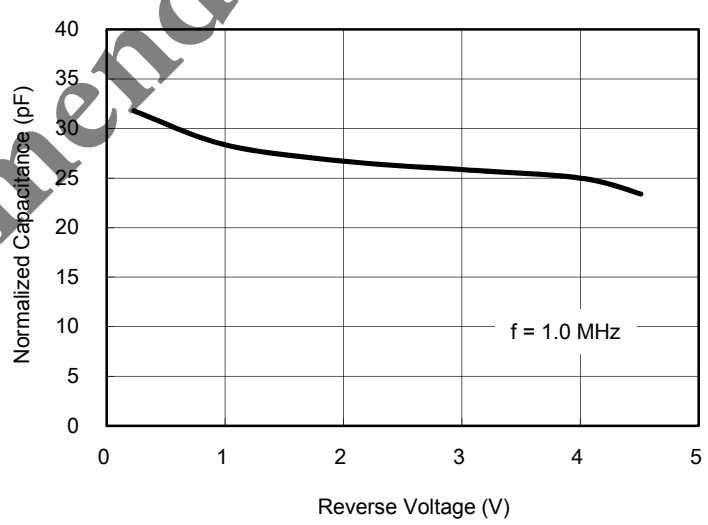
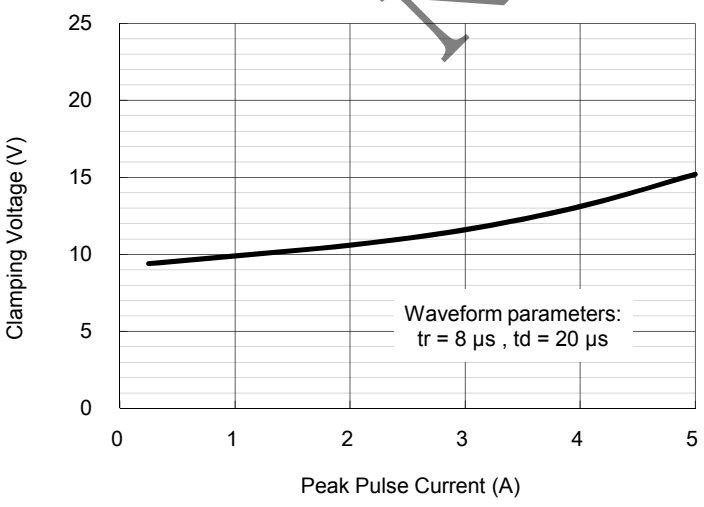


Fig. 5 Clamping Voltage VS. Peak Pulse Current



Small Signal Product

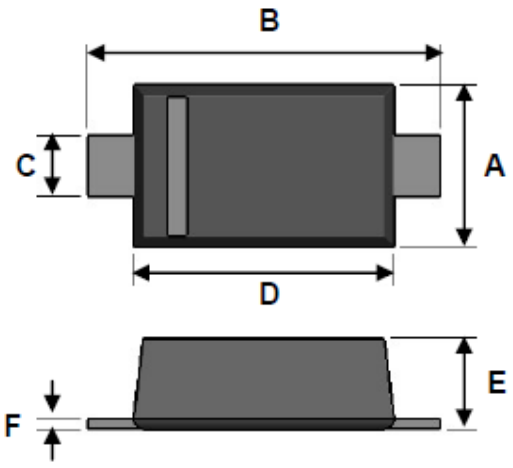
ORDER INFORMATION (EXAMPLE)

TESDD5V0HC RKG

- Green compound code
- Packing code
- Part no.

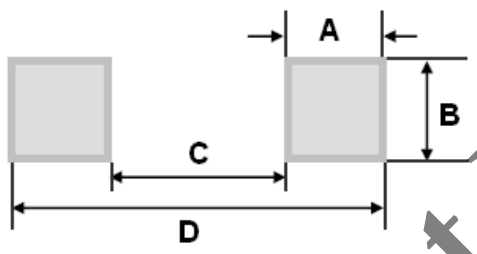
PACKAGE OUTLINE DIMENSIONS

SOD-523F



DIM.	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	0.70	0.90	0.028	0.035
B	1.50	1.70	0.059	0.067
C	0.25	0.40	0.010	0.016
D	1.10	1.30	0.043	0.051
E	0.50	0.77	0.020	0.030
F	0.07	0.20	0.003	0.008

SUGGEST PAD LAYOUT



DIM.	Unit (mm)	Unit (inch)
	Typ.	Typ.
A	0.40	0.016
B	0.40	0.016
C	1.00	0.039
D	1.80	0.071

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

APPLICATION INFROMATION

- Designed to protect one data, I/O, or power supply line
- Designed to protect sensitive electronics from damage or latch-up due to ESD
- Designed to replace multilayer varistors (MLVs) in portable applications
- Offers superior electrical characteristics such as lower clamping voltage and no device degradation when compared to MLVs
- The combination of small size and high ESD surge capability makes them ideal for use in portable applications

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

- Good circuit board layout is critical for the suppression of ESD induced transients
- Place the ESD Protection Diode near the input terminals or connectors to restrict transient coupling
- Minimize the path length between the ESD Protection Diode and the protected line
- Minimize all conductive loops including power and ground loops
- The ESD transient return path to ground should be kept as short as possible

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