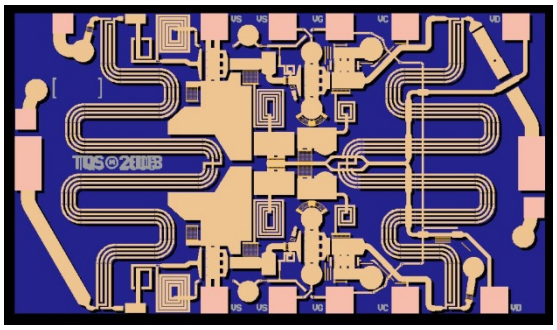
TGA2511

X Band Low Noise Amplifier



Key Features

- Typical Frequency Range: 6 - 14 GHz
- 1.3 dB Nominal Noise Figure
- 20 dB Nominal Gain
- Bias: 5 V, 160 mA Gate Bias
  5 V, 80 mA Self Bias
- 0.15 um 3MI pHEMT Technology
- Chip Dimensions 2.05 x 1.20 x 0.10 mm
  (0.081 x 0.047 x 0.004 in)

Product Description

The TriQuint TGA2511 is a wideband LNA with AGC amplifier for EW, ECM, and RADAR receiver or driver amplifier applications. Offering high gain 20dB typical from 6-14GHz, the TGA2511provides excellent noise performance with typical midband NF 1.3dB, while the balanced topology offers good return loss typically 15dB.

The TGA2511 is designed for maximum ease of use. The large input FETs can handle up to 21dBm input power reliably. The part is also assembled in self-biased mode, using a single +5V supply connection from either side of the chip, or in gate biased mode, allowing the user to control the current for a particular applications.

In self-biased mode the TGA2511 offers 6dBm typical P1dB, while in gate-biased mode the typical P1dB is over 12dBm. The small size of 2.46mm^2 allows ease of compaction into Multi-Chip-Modules (MCMs).

The TGA2511 is 100% DC and RF tested on-wafer to ensure performance compliance.

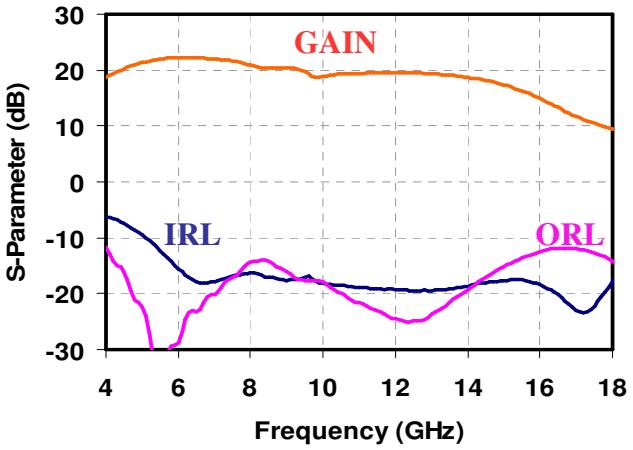
Lead-Free & RoHS compliant.

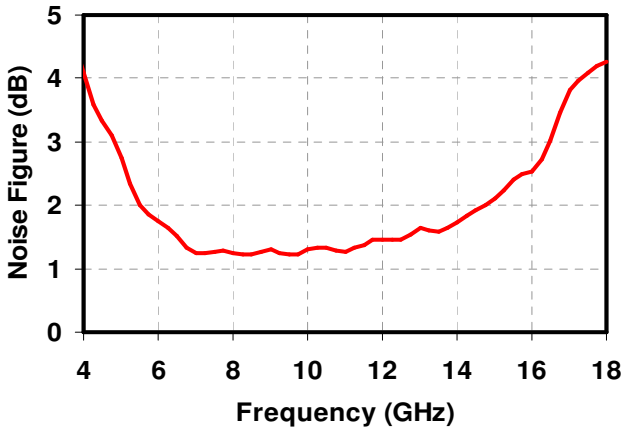
Primary Applications

- X-Band Radar
- EW, ECM
- Point-to-Point Radio

Measured Fixtured Data

Bias Conditions: Gate Bias Vd = 5 V, Id = 160 mA





Datasheet subject to change without notice

TriQuint Semiconductor: www. triquint.com (972)994-8465 Fax (972)994-8504 Info-mmw@tqs.com

TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
Vd	Drain Voltage	Gate Bias: [3.5 + (0.0125)(Id)] V Self Bias: [3.5 + (0.0360)(Id)] V	2/ 3/
Vg	Gate Voltage Range	-1 TO +0.5 V	
Id	Drain Current (gate biased)	240 mA	2/ 4/
|Ig|	Gate Current	14 mA	4/
P_{IN}	Input Continuous Wave Power	21 dBm	
P_D	Power Dissipation	1.56 W	2/ 5/
T_{CH}	Operating Channel Temperature	200 °C	6/ 7/
T_M	Mounting Temperature (30 Seconds)	320 °C	
T_{STG}	Storage Temperature	-65 to 150 °C	

1/ These ratings represent the maximum operable values for this device.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

3/ Unit for Id is mA.

4/ Total current for the entire MMIC.

5/ When operated at this bias condition with a base plate temperature of 70°C, the median life is 3.4E5.

6/ Junction operating temperature will directly affect the device median time to failure (Tm). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

7/ These ratings apply to each individual FET.

TABLE II
DC PROBE TESTS
(Ta = 25 °C, Nominal)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
$V_{BVGS, Q1}$	Breakdown Voltage Gate-Source	-30		-5	V
$V_{P, Q1,2,5,6}$	Pinch-Off Voltage	-0.7		-0.1	V

Q1, Q2, Q5, Q6 are 400 um FET.

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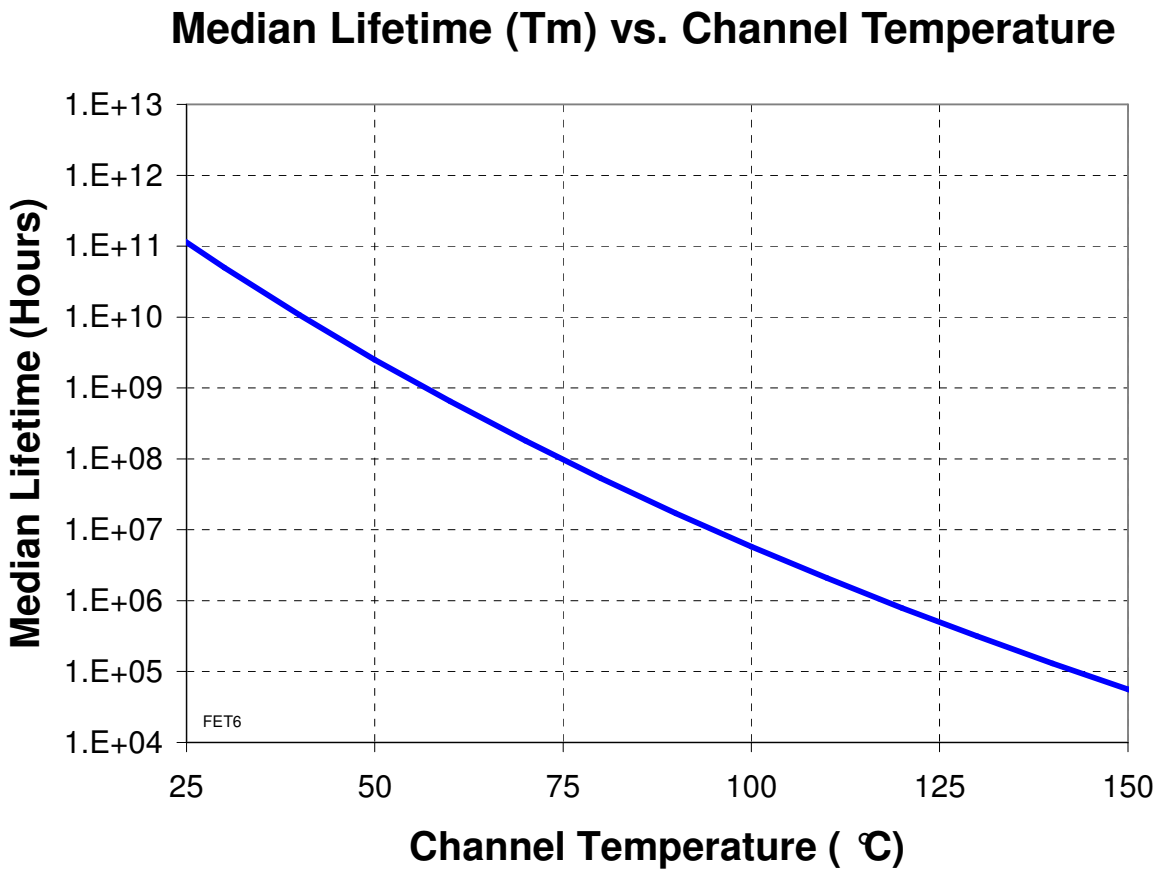
TABLE III
ELECTRICAL CHARACTERISTICS
(Ta = 25 ^{0}C Nominal)

PARAMETER	Gate Bias	Self Bias	UNITS
Frequency Range	6 - 14	6 - 14	GHz
Drain Voltage, Vd	5.0	5.0	V
Drain Current, Id	160	80	mA
Gate Voltage, Vg	-0.1	-	V
Small Signal Gain, S21	20	17	dB
Input Return Loss, S11	18	18	dB
Output Return Loss, S22	18	18	dB
Noise Figure, NF	1.3	1.4	dB
Output Power @ 1dB Gain Compression, P1dB	12	6	dBm
OIP3	24	15	dBm

TABLE IV
THERMAL INFORMATION

PARAMETER	TEST CONDITIONS	T_{CH} (°C)	θ_{JC} (°C/W)	T_m (HRS)
θ_{JC} Thermal Resistance (channel to Case)	Vd = 5 V Id = 160 mA Gate Bias Pdiss = 0.80 W	103.9	42.4	3.8E+6
θ_{JC} Thermal Resistance (channel to Case)	Vd = 5 V Id = 80 mA Self Bias Pdiss = 0.40 W	82.7	31.7	4.1E+7

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70℃ baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.



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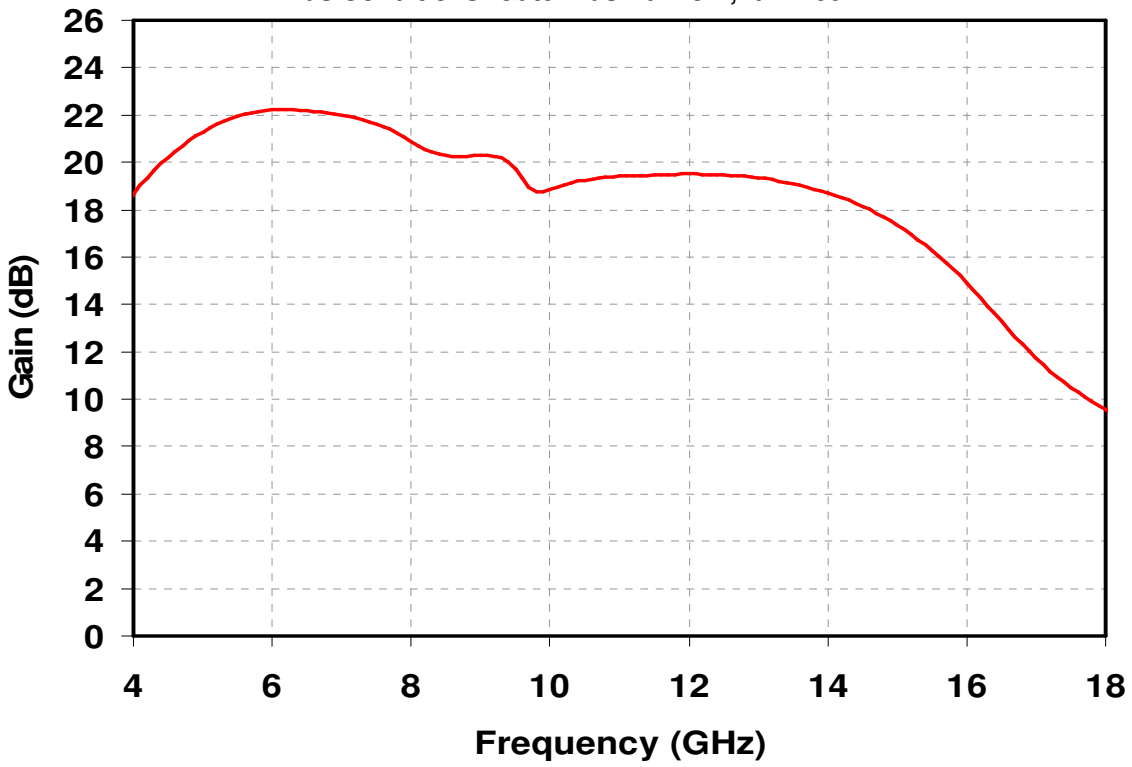
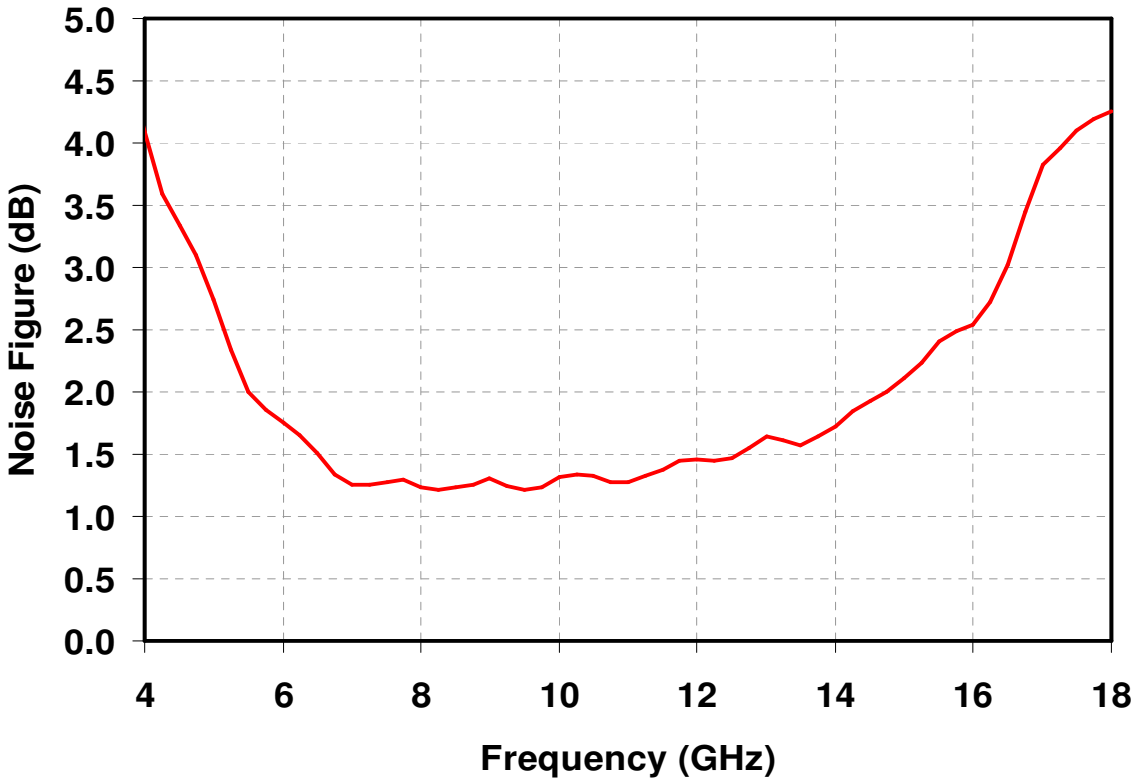
Measured Fixtured Data

Bias Conditions: Gate Bias Vd = 5 V, Id = 160 mA





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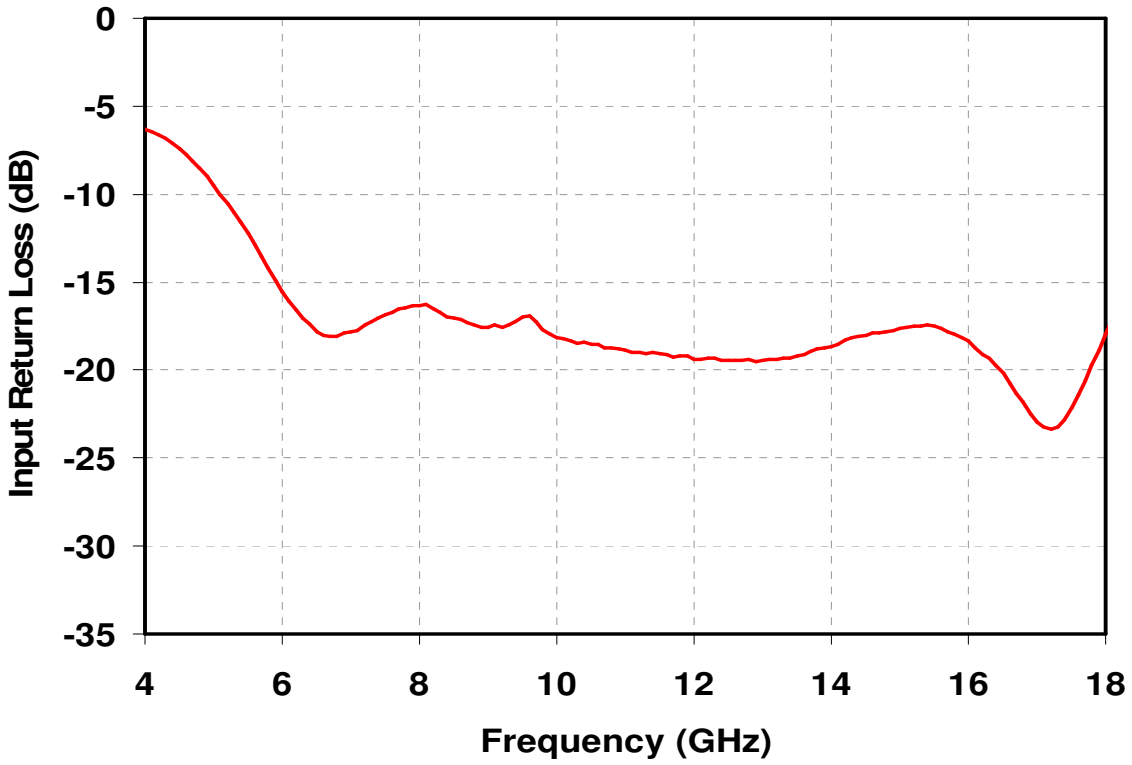

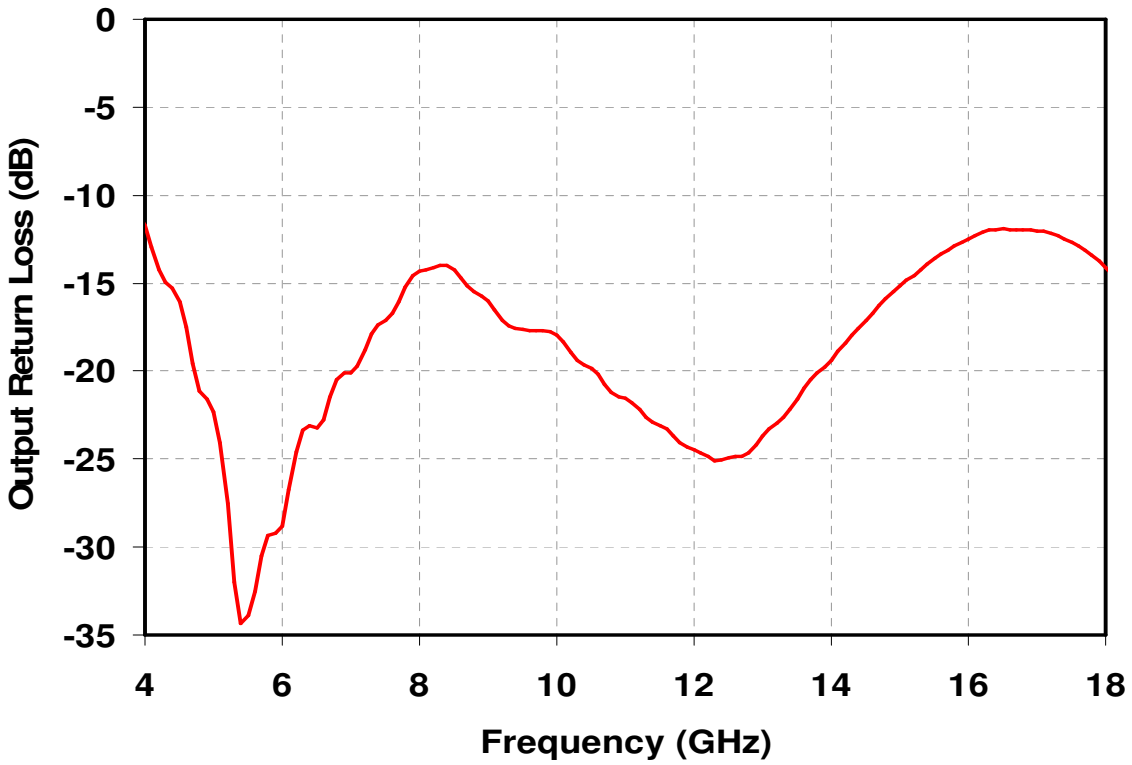

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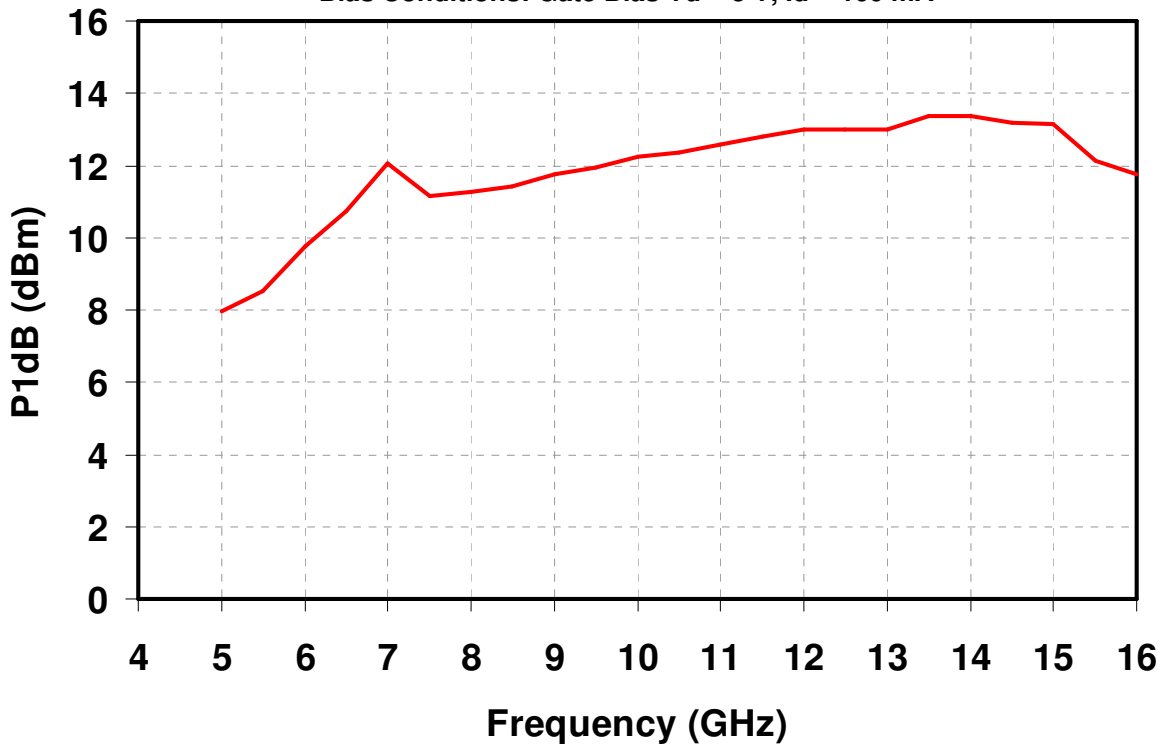
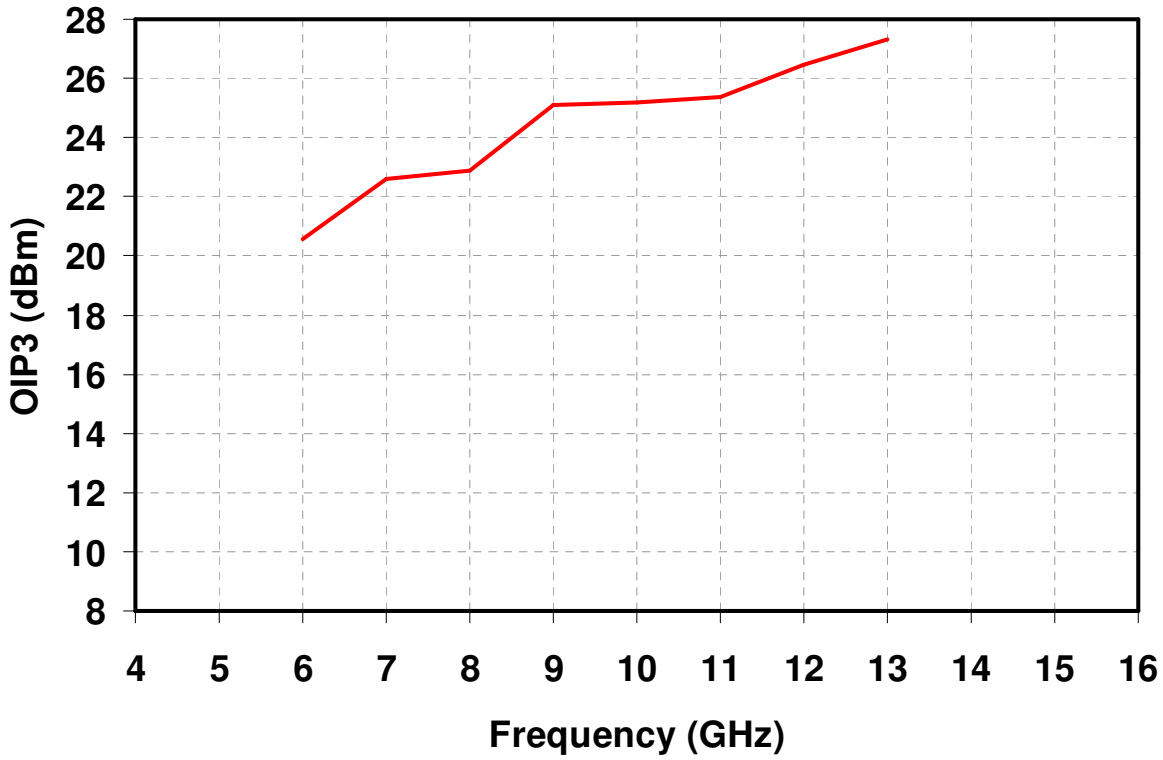
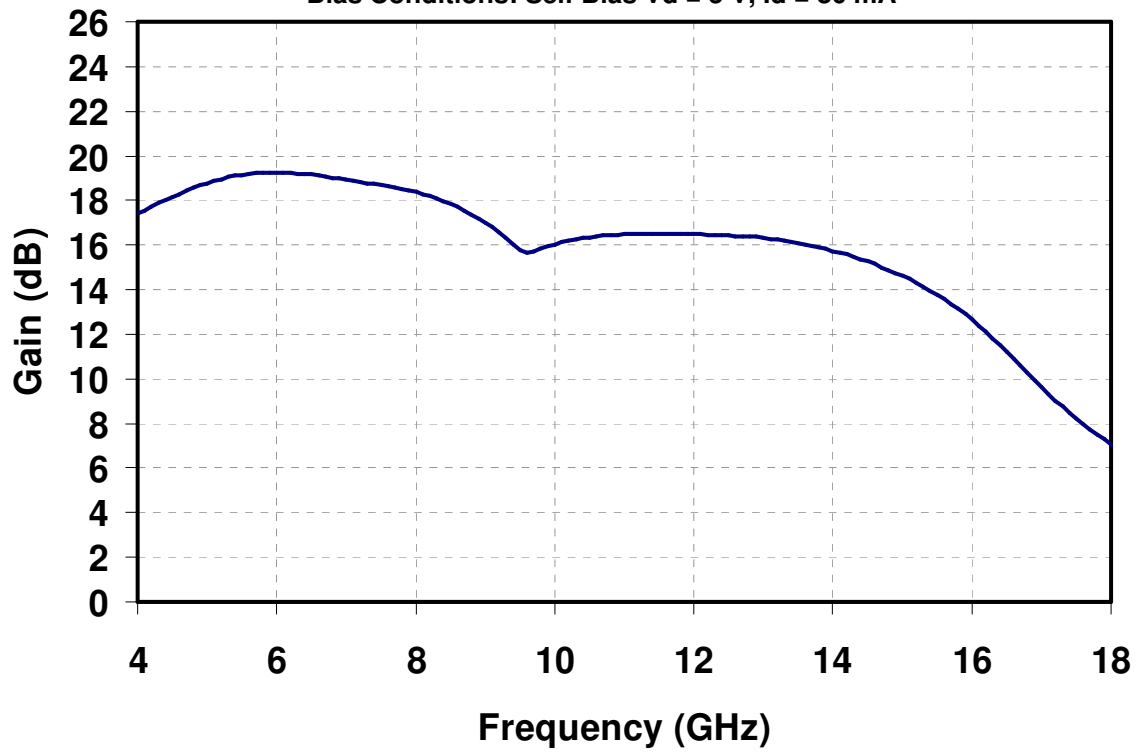
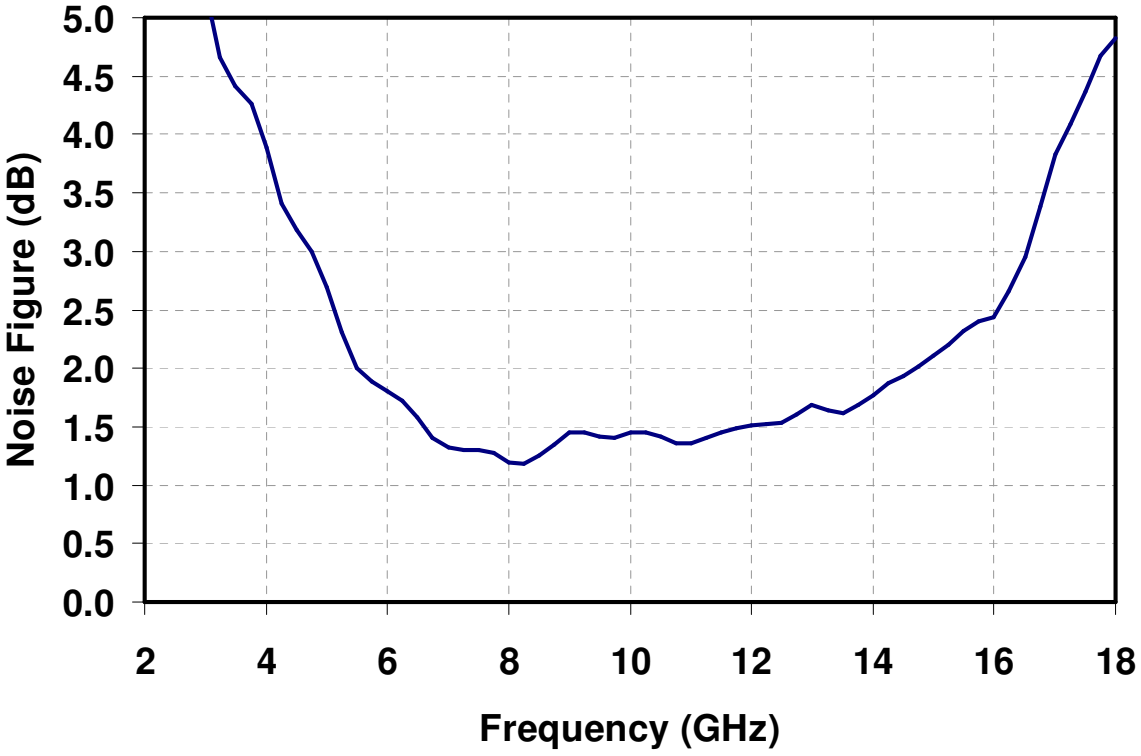




Measured Fixtured Data

Bias Conditions: Self Bias Vd = 5 V, Id = 80 mA





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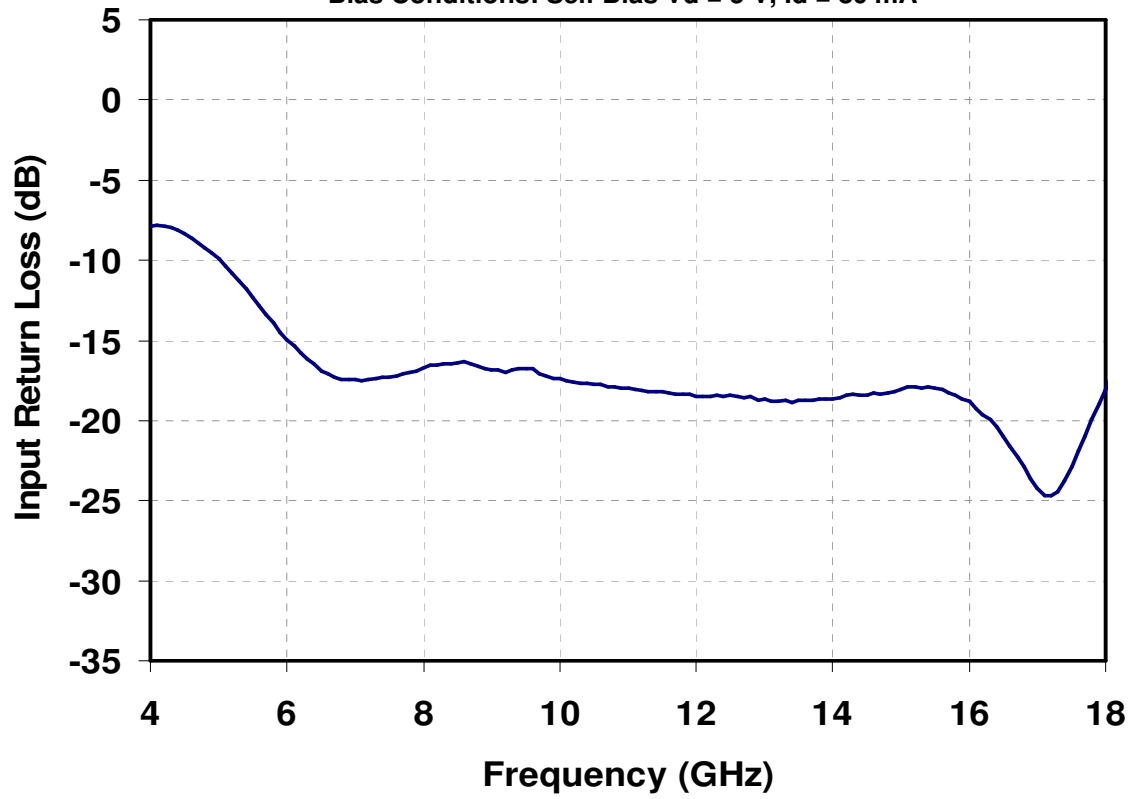

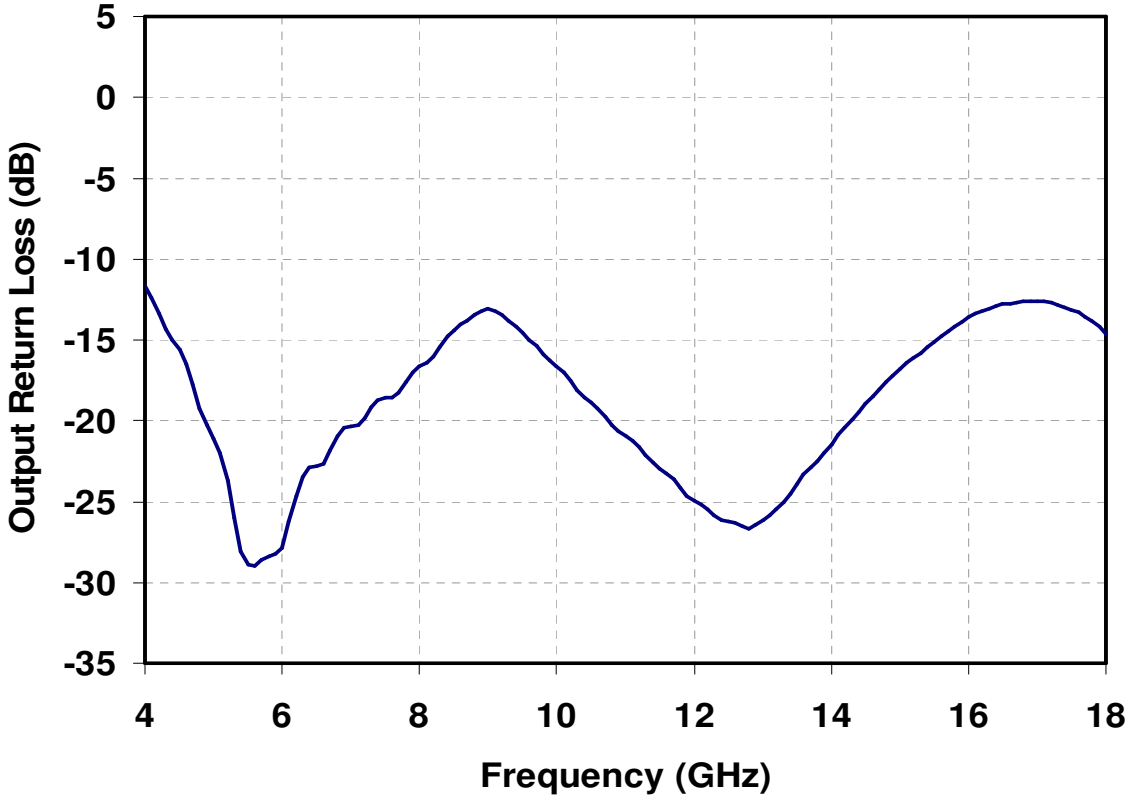

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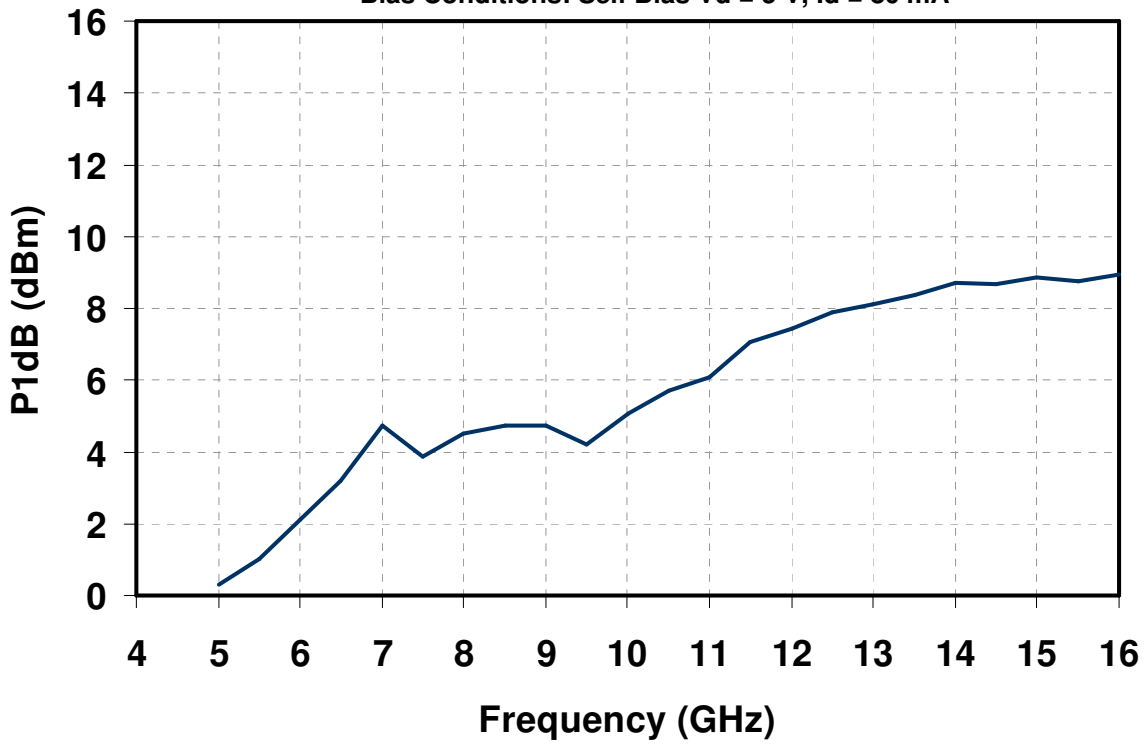
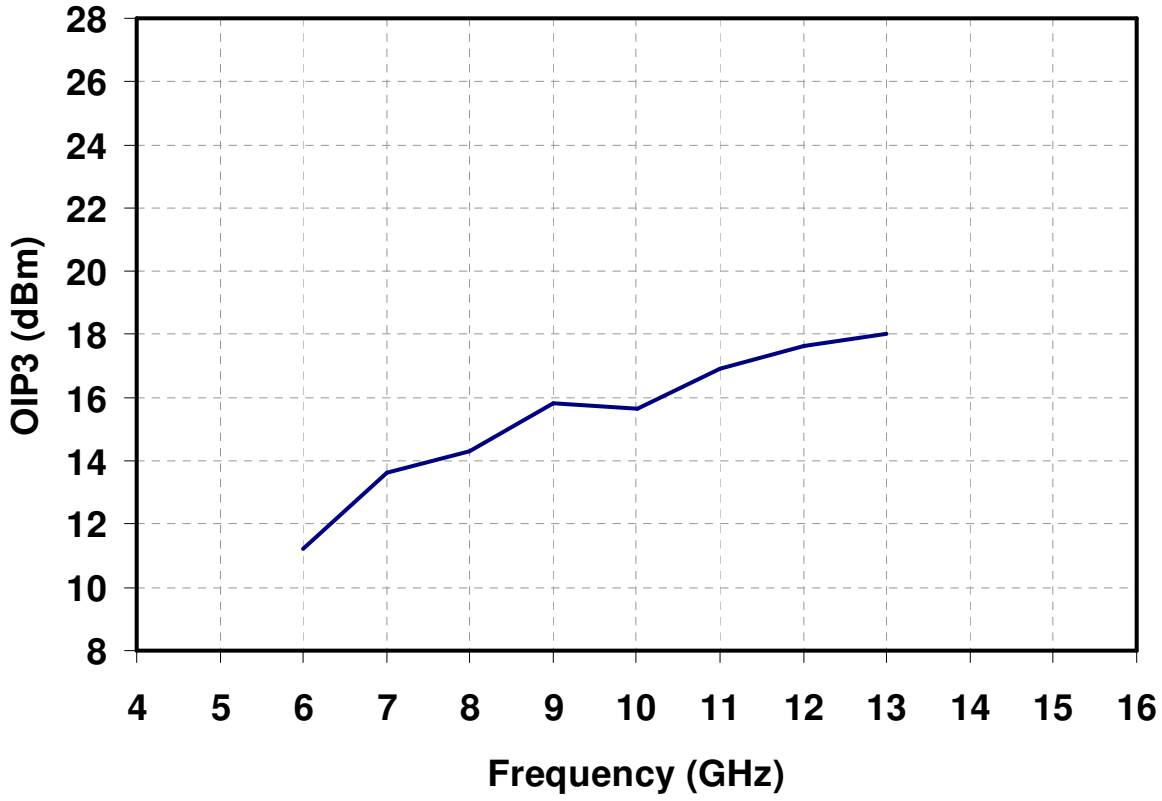
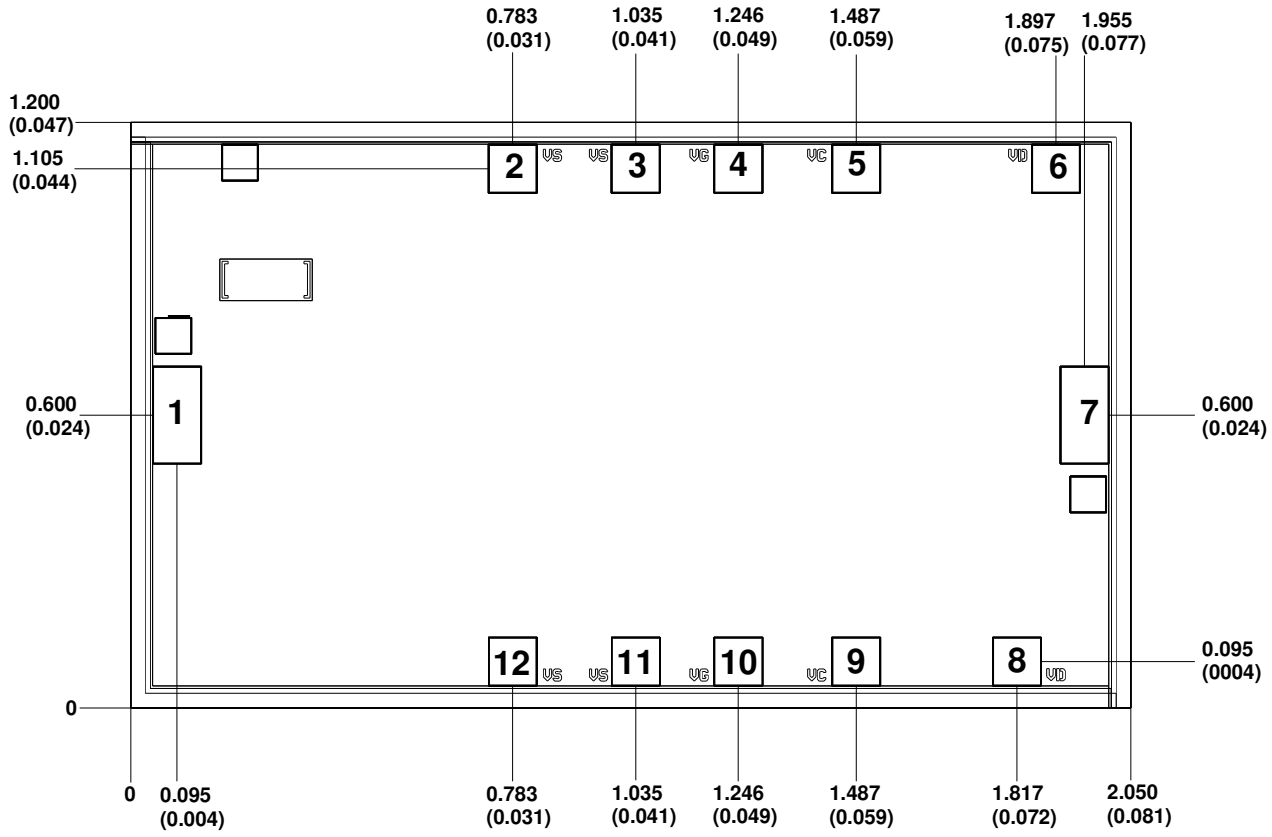




Mechanical Drawing



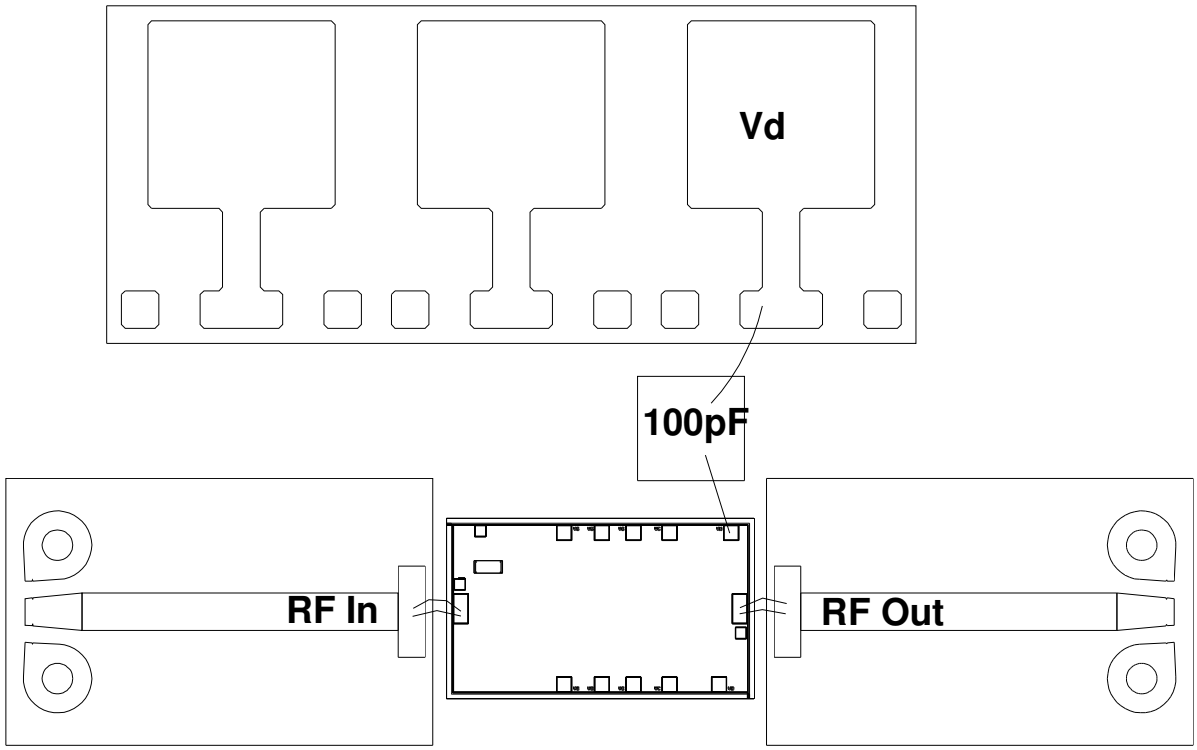
Units: millimeters (inches)
Thickness: 0.100 (0.004)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)
GND is back side of MMIC

Bond pad #1	**(RF In)**	**0.100 x 0.200 (0.004 x 0.008)**
Bond pad #2, 3, 12, 11	**(Vs)**	**0.100 x 0.100 (0.004 x 0.004)**
Bond pad #4, 10	**(Vg)**	**0.100 x 0.100 (0.004 x 0.004)**
Bond pad #5, 9	**(Vctrl)**	**0.100 x 0.100 (0.004 x 0.004)**
Bond pad #6, 8	**(Vd)**	**0.100 x 0.100 (0.004 x 0.004)**
Bond pad #7	**(RF Out)**	**0.100 x 0.200 (0.004 x 0.008)**

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Recommended Chip Assembly Diagram

Option 1: Self Bias - No Gain Control



All DC connections may be brought in from either side of the chip (Use Pad 6 or 8)
0.01uF external Cap is recommended on Drain
Bias: Vd = 5V (Id = ~80mA)

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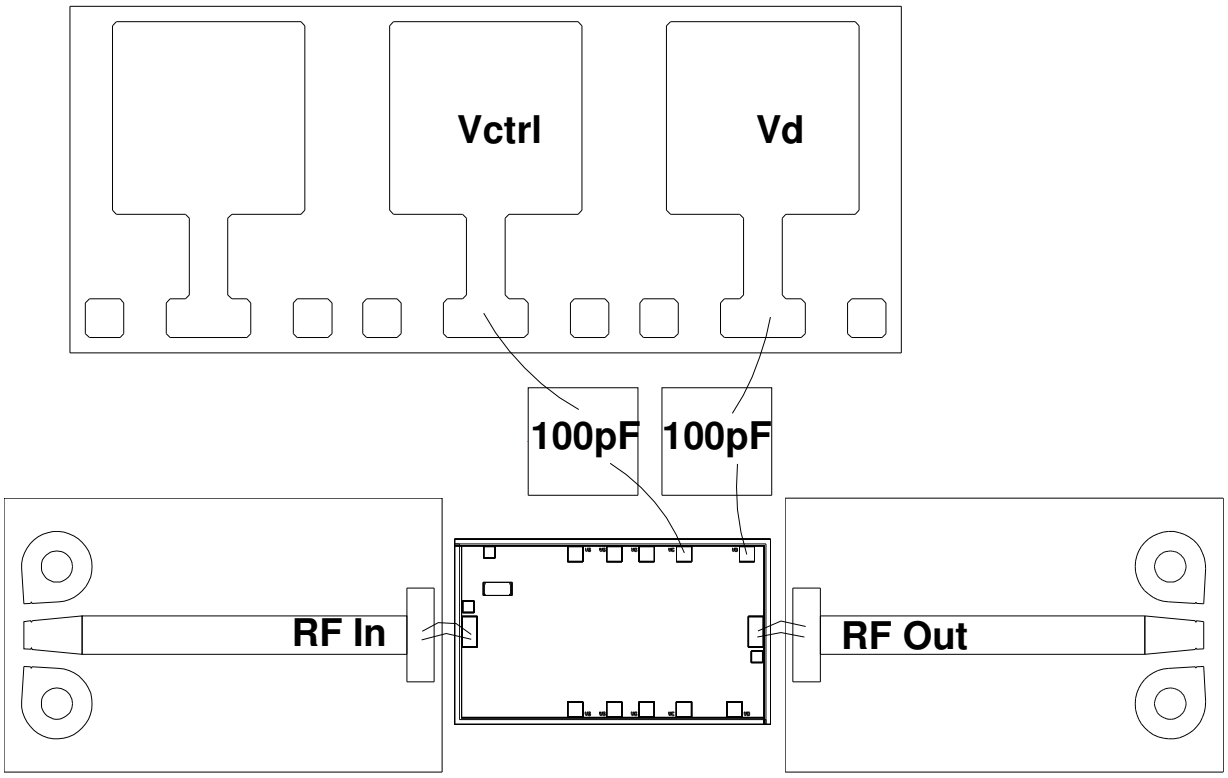
Recommended Chip Assembly Diagram (Con't)

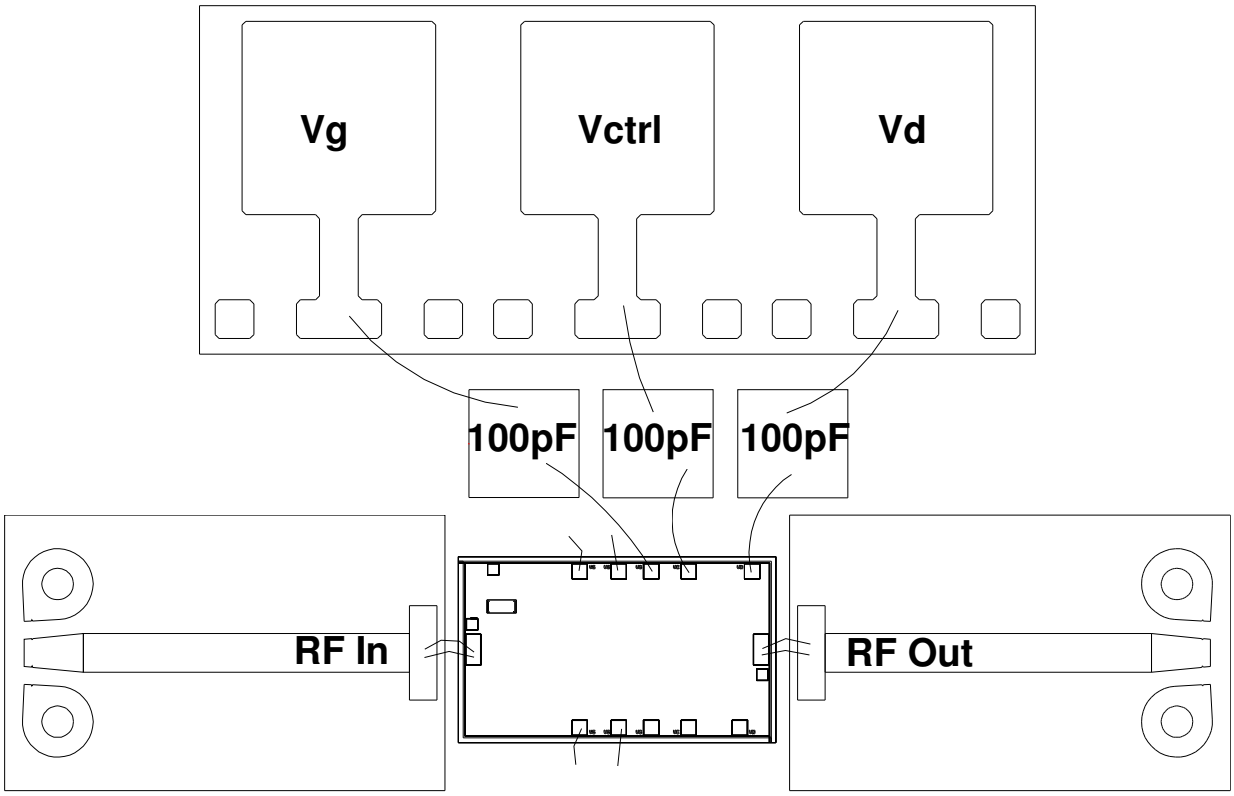
Option 2: Self Bias - With Gain Control



All DC connections may be brought in from either side of the chip (Use Pad 5 or 9, and Pad 6 or 8)
0.01uF external Caps are recommended on Drain line
Bias: Vd = 5V (Id = ~80mA), Vctrl = 0 to +5V for Gain adjustment

Recommended Chip Assembly Diagram (Con't)

Option 3: Gate Bias - With Gain Control



All DC connections may be brought in from either side of the chip (Use Pad 4 or 10, Pad 5 or 9, and Pad 6 or 8)
0.01uF external Caps are recommended on Drain, Gate line, 10 ohm external
series R between 100pF cap and 0.01uF cap is recommended for Gate line
Source connections (Pad 2, 3, 11, 12) are bonded to ground. **All four bond wires are required for stability.**
Bias: Vd = 5V , Vctrl = 0 to +5V for Gain adjustment
Vg = Range, -0.5 to 0, typically ~ -0.1 will provide ~160mA of Id.

Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300^{0}C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200^{0}C.

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