

## Single Line Bi-directional ESD Protection Diode Array UM5052DA DFN2 0.6×0.3

### General Description

The UM5052DA ESD protection diode is designed to replace multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and PDA's. They offer desirable electrical characteristics for board level protection, such as fast response time, lower operating voltage, lower clamping voltage and no device degradation when compared to MLVs. The UM5052DA ESD protection diode protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. The UM5052DA is available in DFN2 0.6mm×0.3mm package with working voltage of 5 volt. It gives designer the flexibility to protect one bidirectional line in applications where arrays are not practical. Additionally, it may be "sprinkled" around the board in applications where board space is at a premium. It may be used to meet the ESD immunity requirements of IEC 61000-4-2, ±30kV air, ±30kV contact discharge.

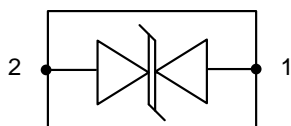
### Applications

- Cell Phone Handsets and Accessories
- Personal Digital Assistants (PDA's)
- Notebooks, Desktops and Servers
- Portable Instrumentation
- Cordless Phones
- Digital Cameras
- Peripherals
- MP3 Players

### Features

- Transient Protection for Data Lines to IEC 61000-4-2 (ESD) ±30kV (Air), ±30kV (Contact)
- Small Package for Use in Portable Electronics
- Suitable Replacement for MLV's in ESD Protection Applications
- Protect One I/O or Power Line
- Low Clamping Voltage
- Stand-off Voltages: 5V
- Low Leakage Current
- Solid-State Silicon-Avalanche Technology

### Pin Configurations



### Top View



**UM5052DA**  
**DFN2 0.6×0.3**

## Ordering Information

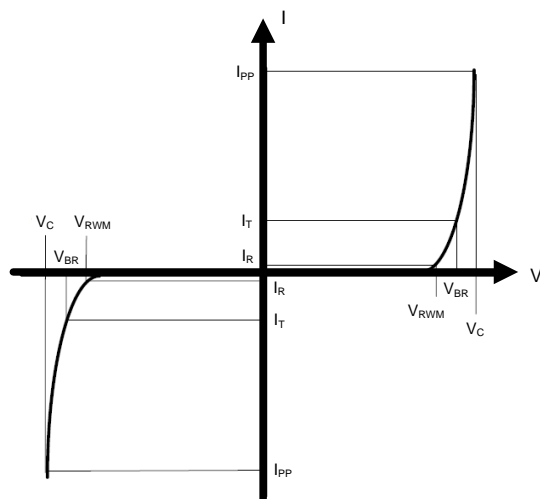
Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM5052DA	5.0V	DFN2 0.6×0.3	1	F	10000pcs/7 Inch Tape & Reel

## Absolute Maximum Ratings

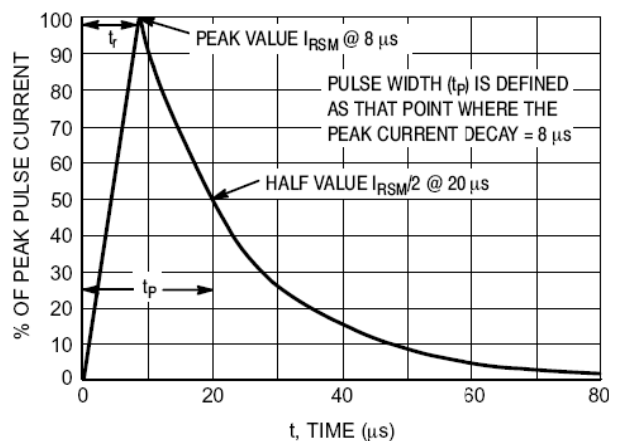
Rating	Symbol	Value	Unit
Peak Pulse Power ( $t_p=8/20\mu s$ )	$P_{PK}$	60	Watts
Maximum Peak Pulse Current ( $t_p=8/20\mu s$ )	$I_{PP}$	5	Amps
Lead Soldering Temperature	$T_L$	260 (10 sec.)	°C
Operating Temperature	$T_J$	-55 to +125	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

## Symbol Definition

Parameter	Symbol
Maximum Reverse Peak Pulse Current	$I_{PP}$
Clamping Voltage @ $I_{PP}$	$V_C$
Working Peak Reverse Voltage	$V_{RWM}$
Maximum Reverse Leakage Current @ $V_{RWM}$	$I_R$
Breakdown Voltage @ $I_T$	$V_{BR}$
Test Current	$I_T$
Peak Power Dissipation	$P_{PK}$
Max. Capacitance @ $V_R=0V, f=1MHz$	$C$



Bi-directional TVS



## Electrical Characteristics

(T = 25 °C, Device for 5.0V Reverse Stand-off Voltage)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	$V_{RWM}$				5	V
Reverse Breakdown Voltage	$V_{BR}$	$I_T=1mA$	6.5	8.0	8.5	V
Reverse Leakage Current	$I_R$	$V_{RWM}=5V, T=25\text{ }^\circ\text{C}$			1	$\mu\text{A}$
Clamping Voltage	$V_C$	$I_{PP}=5A, t_p=8/20\mu\text{s}$		12		V
Junction Capacitance	$C_J$	$V_R=0V, f=1\text{MHz}$		7	10	pF
Junction Capacitance	$C_J$	$V_R=2.5V, f=1\text{MHz}$		6	9	pF

## Applications Information

### Device Connection Options

UM5052DA ESD protection diode is designed to protect one bidirectional data, I/O, or power supply line from the damage caused by ESD and surge pluses. The device is bidirectional and can be used on lines where the signal polarity is above ground and below ground.

### Circuit Board Layout Recommendations for Suppression of ESD

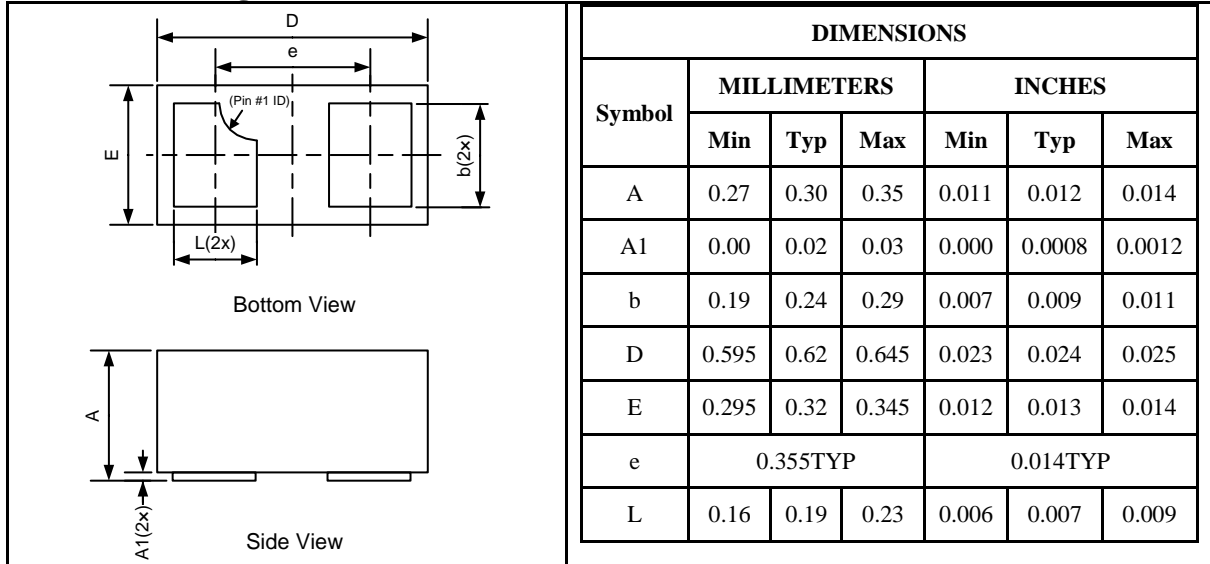
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.
7. Keep parallel signal paths to a minimum.
8. Avoid running protection conductors in parallel with unprotected conductor.
9. Minimize all printed-circuit board conductive loops including power and ground loops.
10. Avoid using shared transient return paths to a common ground point.

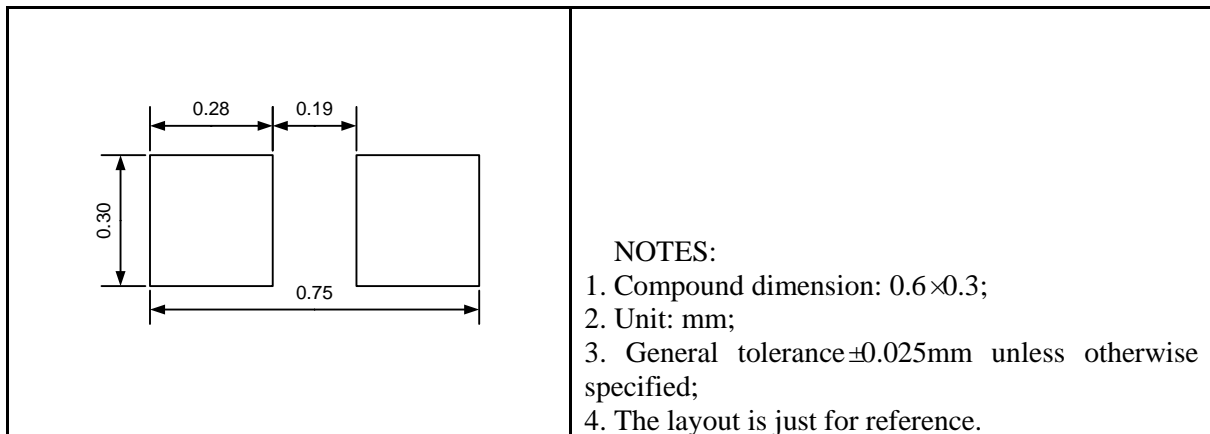
## Package Information

### UM5052DA DFN2 0.6×0.3

#### Outline Drawing



#### Land Pattern



#### Tape and Reel Orientation



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